CAST, Inc.
11 Stonewall Court
Woodcliff Lake, NJ 07677
USA
Phone: +1-201-391-8300
Fax: +1-201-391-8694
E-mail: info@cast-inc.com
URL: www.cast-inc.com

Features
- Available under terms of the SignOnce IP License
- ISO/IEC 15444-1 JPEG 2000 Image Coding System compliance
- Both lossless and lossy compression
- Error-resilient compression
- Rate control
- Headers syntax
- Performs both Tier-1 and Tier-2 operations; external processing not required
- Flexible Input Image Format:
  - Sub-sampling factors up to four for each component
  - Image/Tile size up to 4096x4096.
  - Up to four color components
  - Eight up to fourteen bits per sample
- Output format:
  - Proprietary attributes/coded data format
  - Standard compliant stream (.jpc)
  - Standard compliant file (.jp2)
- Programmable JPEG 2000 options
  - 2D-DWT filter type (5/3 or 9/7)
  - Number of 2D-DWT levels
  - Quantization tables

Table 1: Example Implementation Statistics for Xilinx® FPGAs

<table>
<thead>
<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax</th>
<th>Slices</th>
<th>IOb</th>
<th>GCLK</th>
<th>BRAM</th>
<th>MULT</th>
<th>External Memory</th>
<th>Supported Video Format</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex™-4</td>
<td>XC4VFX80-12</td>
<td>100</td>
<td>27161</td>
<td>255</td>
<td>1</td>
<td>120</td>
<td>36</td>
<td>21.4</td>
<td>HD 720p, 30 fps</td>
<td>ISE™8.2.03i</td>
</tr>
<tr>
<td>Virtex™-5</td>
<td>XC5VLX85-3</td>
<td>120</td>
<td>11598</td>
<td>255</td>
<td>1</td>
<td>62</td>
<td>18</td>
<td>21.4</td>
<td>HD 720p, 30 fps</td>
<td>ISE™9.1.03i</td>
</tr>
</tbody>
</table>

Notes:
1) Results are only indicative as the core can be configured for higher/lower processing speed and higher/lower frame format support.
2) Assuming all core I/Os and clocks are routed off-chip.
Figure 1: JPEG2K-E Function Controller Block Diagram

Features (continued)
- Entropy-coding switches (reset, restart, segmark)
- Input format (pixel depth, image/tile size, number of components, sub-sampling factors)
- Code-block size (64 or 32 or 16 on each dimension)
- Target compression ratio
- Architecture can be tuned during synthesis
  - Configurable number of Entropy Coding Units
  - Configurable maximum image/tile size
- Flexible Interfaces
  - 16-bit synchronous SRAM-style host interface
  - Dedicated pixel-in and stream-out interfaces
- Flexible, external memory interface, independent of memory type - supporting SRAM, SDR SDRAM, DDR/DDR2, SDRAM, and DQR SRAM - pin compatible with CAST’s memory controller cores
- Fully synchronous single-clock domain design
- Sophisticated self-checking
- Bit accurate model in C

Applications
- Satellite, military, and other extreme surveillance systems
- Medical and other highest-quality video and image systems
- Digital still cameras and camcorders
- Networked video and image distribution systems
- Wireless video and image distribution systems
- Digital CCTV and surveillance systems
- Image and Video editing systems
General Description

The JPEG2K-E core is a complete, high-performance JPEG 2000 (ISO/IEC 15444-1) image compression solution targeted for video and high-bandwidth image compression applications. The core implements both Tier-1 and Tier-2 JPEG 2000 encoding — including rate control — in efficient custom hardware. Once programmed, the core operates independently to receive pixel data and output a fully-compliant video stream at the desired compression ratio. It can process individual frame or tile sizes up to 4096 x 4096 pixels, depending only on the external memory provided. Its high-performance processing achieves rates over 200 MSamples/sec in ASICs and over 100 MSamples/sec in FPGAs. This competitive capacity and speed eliminate the need for parallel processing for even the most demanding applications such as HDTV.

The JPEG2K-E is a reliable and easy-to-integrate core as it is carefully designed, and rigorously verified. A complete verification environment eases integration, and a software bit-accurate model plus additional aids for system-on-chip simulation are included.

Functional Description

The JPEG2K-E operates either on an entire image or on a rectangular section of an image called a tile. The maximum supported image or tile size depends on the size of the external memory. With enough external memory, the core can support up to 4096x4096 images. The core implements a simple and flexible external memory interface, making JPEG2K-E independent of memory type—supporting SRAM, SDR and DDR SDRAM, or QDR SRAM. The JPEG2K-E consists of several functional blocks, as shown in the block diagram and briefly explained here.

As encoding begins, the input pixels are first level-shifted and then transformed using either the reversible 5/3 or the irreversible 9/7 two-dimensional discrete wavelet transform. The transformed coefficients are stored in the external memory.

After an entire tile has been transformed, the transformed coefficients are quantized. The quantized coefficients are fed to the Entropy Coding Engines in a code-block per code-block basis.

The coded-segments along with the code-block attributes (truncation lengths and distortion metrics) produced by the Entropy Coding Engines are fed to the Rate Control Engine. If enabled, the Rate Control Engine implements a proprietary PCRD algorithm that outputs a code-stream at the required compression ratio with the minimum possible loss of quality.

Finally the Headers-Syntax Unit forms global, tile and packet headers, and outputs a compliant stream or file. This may be omitted from the core if it is not needed.

Core Modifications

JPEG2k_E can be modified so that it fits almost any applications needs in terms of processing speed. This is achieved by instantiating 1, 3, 6, 9 or 12 entropy-coding units. Furthermore, modifications regarding the core interface are also feasible.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.
Table 2: Core I/O Signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Signal Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Input</td>
<td>Clock</td>
</tr>
<tr>
<td>rst</td>
<td>Input</td>
<td>Asynchronous reset</td>
</tr>
<tr>
<td>clr</td>
<td>Input</td>
<td>Synchronous clear</td>
</tr>
<tr>
<td>h_select</td>
<td>Input</td>
<td>Core select</td>
</tr>
<tr>
<td>h_r_wb</td>
<td>Input</td>
<td>Transfer direction</td>
</tr>
<tr>
<td>h_addr[7:0]</td>
<td>Input</td>
<td>Address bus</td>
</tr>
<tr>
<td>h_data_in[15:0]</td>
<td></td>
<td>Write data bus</td>
</tr>
<tr>
<td>h_w_rdy</td>
<td>Output</td>
<td>Write ready: Core available for write</td>
</tr>
<tr>
<td>h_data_out_v</td>
<td>Output</td>
<td>Read data valid</td>
</tr>
<tr>
<td>h_data_out[15:0]</td>
<td></td>
<td>Read data bus</td>
</tr>
<tr>
<td>i_pixel_v</td>
<td>Input</td>
<td>Pixel indicator. Indicates that pixel data reside in the i_data bus.</td>
</tr>
<tr>
<td>i_header_v</td>
<td>Input</td>
<td>Header indicator. Indicates that header/comment data reside in the i_data bus.</td>
</tr>
<tr>
<td>i_data[15:0]</td>
<td>Input</td>
<td>Input data bus</td>
</tr>
<tr>
<td>i_data_rdy</td>
<td>Output</td>
<td>Data ready. Indicates that the core is ready to accept data.</td>
</tr>
<tr>
<td>s_data_rdy</td>
<td>Input</td>
<td>Stream ready. Indicates to the core that it can output stream data</td>
</tr>
<tr>
<td>s_data[15:0]</td>
<td>Output</td>
<td>Stream data bus</td>
</tr>
<tr>
<td>s_data_v</td>
<td>Output</td>
<td>Stream data valid. Mask valid data in output stream data.</td>
</tr>
<tr>
<td>s_sot</td>
<td>Output</td>
<td>Start of tile. Masks first word of a stream corresponding to a tile.</td>
</tr>
<tr>
<td>s_eot</td>
<td>Output</td>
<td>End of tile. Masks last word of a stream corresponding to a tile.</td>
</tr>
<tr>
<td>busy</td>
<td>Output</td>
<td>Busy. Indicates that the core is busy processing image data.</td>
</tr>
<tr>
<td>cfg_error</td>
<td>Output</td>
<td>Configuration error. Indicates that some erroneous value has been found in the configuration registers.</td>
</tr>
<tr>
<td>xmem_clk</td>
<td>Input</td>
<td>Clock</td>
</tr>
<tr>
<td>xmem_rst</td>
<td>Input</td>
<td>Asynchronous reset line of the xmem_clk clock domain.</td>
</tr>
<tr>
<td>xmem_clr</td>
<td>Input</td>
<td>Synchronous reset line of the xmem_clk clock domain.</td>
</tr>
<tr>
<td>xmem_req_rdy</td>
<td>Input</td>
<td>Memory controller ready to receive a new request.</td>
</tr>
<tr>
<td>xmem_req_val</td>
<td>Output</td>
<td>Access request valid.</td>
</tr>
<tr>
<td>xmem_req[SP:0](^1)</td>
<td>Output</td>
<td>Access request.</td>
</tr>
<tr>
<td>xmem_wdata_rdy</td>
<td>Input</td>
<td>Memory controller ready to receive new write data.</td>
</tr>
<tr>
<td>xmem_wdata_val</td>
<td>Output</td>
<td>Write data valid.</td>
</tr>
<tr>
<td>xmem_wdata [15/31/63/127:0](^1)</td>
<td>Output</td>
<td>Write data.</td>
</tr>
<tr>
<td>xmem_wdata_mask</td>
<td>Output</td>
<td>Write data mask (1 bit per 16bit1 in the xmem_wdata bust).</td>
</tr>
<tr>
<td>xmem_rdata_rdy</td>
<td>Output</td>
<td>Core ready to receive new read data.</td>
</tr>
<tr>
<td>xmem_rdata_val</td>
<td>Input</td>
<td>Read data valid.</td>
</tr>
<tr>
<td>xmem_rdata [15/31/63/127:0](^1)</td>
<td>Input</td>
<td>Read data.</td>
</tr>
</tbody>
</table>

\(^1\) Configurable during synthesis

February 21, 2008
Verification Methods
The core has been verified through extensive simulation and rigorous code coverage measurements. The SDF model of the core has been fed with a number of images that have been efficiently decoded by the standard’s reference software and the common Kakadu software. Furthermore, the core has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Recommended Design Experience
The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information
This product is available directly from Xilinx AllianceCORE member CAST, Inc. under the terms of the SignOnce IP License. Please contact CAST for pricing and additional information about this product. Contact information for them is on the front page of this datasheet. The JPEG2K-E core is licensed from Alma Technologies, S.A. To learn more about the SignOnce IP License program, contact CAST or visit the web:

- Email: commonlicense@xilinx.com
- URL: www.xilinx.com/ipcenter/signonce

Related Information
Industry Information

Xilinx Programmable Logic
For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

- Xilinx, Inc.
  2100 Logic Drive
  San Jose, CA 95124
  Phone: +1 408-559-7778
  Fax: +1 408-559-7114
  URL: www.xilinx.com

For AllianceCORE™ specific information: