



## 2018 Xilinx Security Working Group (XSWG) Munich, Germany Agenda

Hilton Airport Munich, Terminalstraße Mitte 20, 85356 München-Flughafen, Germany

<b>Tuesday, December 18, 2018</b>	
<b>All Lectures in Munich I + II Room</b>	
<b>Topic</b>	<b>Time</b>
Check In and Continental Breakfast	7:15 - 8:15
Welcome / Introduction to Xilinx Security	8:15 - 8:45
Next Generation Security / Survey	8:45 - 10:00
Break	10:00 - 10:30
Versal Introduction / Security Enhancements	10:30 - 11:45
Lunch	11:45 - 12:45
Versal Security Use Cases	12:45 - 1:45
Break	1:45 - 2:15
Versal Secure Boot	2:15 - 3:45
Break	3:45 - 4:15
Guidance on Essential Security Design Resources/Information	4:15 - 5:00
Day 1 Wrap Up / Summary Statements	5:00 - 5:15
Evening Social and Partner Demonstrations	5:30 - 7:30



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Wednesday, December 19, 2018		
Check In and Continental Breakfast		7:45 - 8:15
Lectures :Munich I + II Room	Time	Demonstrations : Tokyo / Istanbul Room
All Hands Day 2 Re-Greet	8:15 - 8:30	(No Demo This Period)
Zynq UltraScale+ MPSoC Security	8:30 - 9:00	UltraScale and UltraScale+ FPGA Secure Configuration
	9:00 - 9:30	UltraScale and UltraScale+ FPGA Tamper Logging and Penalty Response
Break	9:30 - 10:00	Break
Zynq UltraScale+ MPSoC Secure Boot	10:00 - 11:00	Functional and Physical Isolation Within the Programmable Logic (PL) of the Zynq UltraScale+ MPSoC
Zynq UltraScale+ MPSoC Trusted Execution Environment	11:00 - 12:00	Functional and Physical Isolation Within the Processing Subsystem (PS) of the Zynq UltraScale+ MPSoC
Lunch	12:00 - 1:00	Lunch
Security in Automotive Applications	1:00 - 2:00	Zynq UltraScale+ MPSoC Secure Boot
Security in Industrial IoT	2:00 - 3:00	
Break	3:00 - 3:30	Break
Security Monitor (SecMon) IP	3:30 - 4:00	Zynq UltraScale+ MPSoC Enhanced Key Revocation
	4:00 - 4:30	Secure Storage Using the Zynq UltraScale+ MPSoC Physical Unclonable Function (PUF)
Next Generation Survey Results	4:30 - 5:00	(No Demo This Period)
XSWG 2018 Adjournment	5:00 - 5:15	