



(Preliminary Agenda) 2019 Functional Safety Working Group (FSWG)

Hilton Munich Airport, Terminalstrasse Mitte 20, 85356, Munich, Germany

Day 1 June 26, 2019		
Topic	Presenter	Time
Check In 7:15 / Continental Breakfast		7:15 - 8:00 AM
Welcome/Introduction/Logistics	Pramod Bhardwaj Xilinx	8:00 - 8:15 AM
State of the Union	Pramod Bhardwaj Xilinx	8:15 - 8:45 AM
General Quality, Reliability and Safety	Krimo Semmoud Xilinx	8:45 - 9:15 AM
Break		9:15 - 9:30 AM
SEU Strategy	Karsten Trott Xilinx	9:30 - 10:15 AM
ZU+ Transient Failure Analysis	Oscar Ballan Xilinx	10:15 - 10:45 AM
Development Tools Certification (ZU+, Versal)	Krimo Semmoud Xilinx	10:45 - 11:15 AM
ZU+ Safety Concept / Architecture	Pramod Bhardwaj Xilinx	11:15 - 12:00 AM
Lunch		12:00 - 1:00 PM
ZU+ HW Safety Mechanism Deep Dive	Oscar Ballan Xilinx	1:00 - 2:00 PM
ZU+ SW Safety Mechanism Deep Dive	Pramod Bhardwaj Xilinx	2:00 - 3:00 PM
Break		3:00 - 3:15 PM
ZU+ DFA/CCF Analysis	Oscar Ballan Xilinx	3:15 - 4:15 PM
FMEDA Calculation	Oscar Ballan Xilinx	4:15 - 5:15 PM
Day One Wrap Up	Xilinx	5:15 - 5:30 PM
June 26, 2019 : Day 1 Social		
Join us for light appetizers and cocktails		5:15 - 7:30 PM



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Day 2 June 27, 2019		
Topic	Presenter	Time
Re-Check In 7:30 / Continental Breakfast		7:30 - 8:00 AM
Security in Functional Safety	Jim Wesselkamper Xilinx	8:00 - 9:00 AM
Design Flows for Functional Safety	Jim Wesselkamper Xilinx	9:00 - 10:00 AM
Break		10:00 - 10:15 AM
PL Isolation: Walk-through Lab	Pramod Bhardwaj Xilinx	10:15 - 11:15 AM
PS Isolation: Walk-through Lab	Jim Wesselkamper Xilinx	11:15 - 12:15 PM
Lunch		12:15 - 1:15 PM
ZU+ PMU Firmware and STL Design Example	Pramod Bhardwaj Xilinx	1:15 - 2:15 PM
ZU+ Functional Safety Design Example	Pramod Bhardwaj Xilinx	2:15 - 3:15 PM
Break		3:15 - 3:30 PM
Xilinx Functional Safety Solutions Roadmap (Versal, STLs, ASIL D)	Multiple	3:30 - 5:00 PM
FSWG Adjournment and Call to Action	Xilinx	5:00 - 5:15 PM