Rapid Development of Video/Imaging Systems

Build real-time video and imaging applications quickly and easily with the Xilinx Video Starter Kit.

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Advances in media encoding schemes are enabling a broad array of applications, including digital video recorders (DVRs), network surveillance cameras, medical imaging, digital broadcasting, and streaming set-top boxes. The promise of streaming media presents a series of implementation challenges, especially when processing complex compression algorithms such as MPEG-4 and MPEG-compressed video transcoding. Given the high computational horsepower required for encoding or decoding such complex algorithms, achieving optimal balance of power, performance, and cost is a significant challenge for streaming media devices.

By using FPGAs, you can differentiate your standard-compliant systems from your competitor's products and achieve the optimal balance for your application. With the MPEG-4 compression scheme, for example, it is possible to offload the IDCT (inverse discrete cosine transform) portion of the algorithm from an MPEG processor to an FPGA to increase the processing bandwidth. IDCT (and DCT at the encoder) can be implemented extremely efficiently using FPGAs, and optimized IP cores are readily available to include in MPEG-based designs.

By integrating various IP cores together with the IDCT core, you can develop a low-cost, single-chip solution that increases processing bandwidth and gives higher quality images than your competitor's ASSP-based solution.

To help you accelerate your system design, Xilinx offers the Video Starter Kit (VSK) 4VSX35. The VSK is an all-digital platform for real-time video/image acquisition, processing, and display. It integrates the power of hardware-accelerated processing as well as an embedded PowerPC™ core for the transmission of high-resolution digital video over lower bandwidths, or for processing network protocol stack and control functions.

Xilinx Video Starter Kit 4VSX35

The Xilinx® VSK 4VSX35 allows you to jump-start your high-performance audio, video, and imaging processing designs. At the heart of the VSK are two highly programmable Xilinx FPGAs (XC2VP4 and XC4VSX35), video encoder, video decoder, AC97 CODEC, and a wide range of video interfaces.

Figure 1 illustrates the VSK's primary components, peripherals, and available I/O.

The VSK comprises three major hardware components: a Xilinx ML402-SX35 board; 752 x 480-pixel RGB progressive scan CMOS image-sensor camera with a frame rate as high as 60 frames per second (fps); and video I/O daughtercard (VIODC). The VIODC is connected to the ML402-SX35 board through the Xilinx Generic Interface (XGI), while the CMOS camera is connected to the VIODC through the serial LVDS interface.

The video encoder is a high-speed, video digital-to-analog converter. It has three separate 10-bit-wide input ports that accept data in high- or standard-definition video formats. It also controls the insertion of appropriate synchronization signals; external horizontal, vertical, and blanking signals; or EAV/SAV timing codes for all standards.

The video decoder is a high-quality, single-chip, multi-format video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video into a digital ITU-R BT.656 format. The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked clock-based systems. This makes the VSK ideally suited for a broad range of applications with diverse video characteristics, including broadcast sources, security and surveillance cameras, and professional video systems. Figure 2 shows a block diagram of the Video Starter Kit.

With the video encoder, video decoder, DVI receiver, DVI transmitter, and camera supporting a two-wire serial I^2C-compatible interface, all of these devices can be controlled through an I^2C master core located either in the XC4VSX35 or XC2VP4 device.

The flexibility of the VSK architecture makes it suitable as a development platform for a variety of multimedia, video, and imaging applications, which include:

- Medical imaging
- Home media gateways
- Multi-channel digital video recorders
- IP TV set-top boxes
- Video-on-demand servers
- Digital TV
- Digital camera and camcorders
- A/V broadcasts
- Network surveillance cameras

System Generator for DSP v8.1

Converting image processing algorithms to FPGA implementations can be challenging, as the algorithms may be proven in software but not directly linked to the actual implementation. Additionally, it can be difficult to subjectively verify the implementation.

Xilinx System Generator for DSP allows for high-level mathematical verification and converts the heart of the algorithm into ready-to-use HDL, which bridges the gap from the algorithm developer to the FPGA engineer.

Using System Generator and the VSK to develop and implement image-processing algorithms allows for a thoroughly verified and easily executed design. The high-level block diagram allows for easy communication between team members, resulting in less time spent crossing skill boundaries when determining implementation trade-offs.

Figure 1 - Video Starter Kit 4VSX35

To accelerate video/imaging system development, Xilinx has developed new System Generator blocks specifically for the VSK, including:

- VIODC interface block
- Multi-port DDR memory controller block
- System-level blocks

With these pre-tested blocks, you can easily build your video/imaging system by just dragging and dropping the blocks within System Generator to construct your system, saving precious time from coding these essential interfacing blocks in HDL.

To be able to handle the enormous video data stream

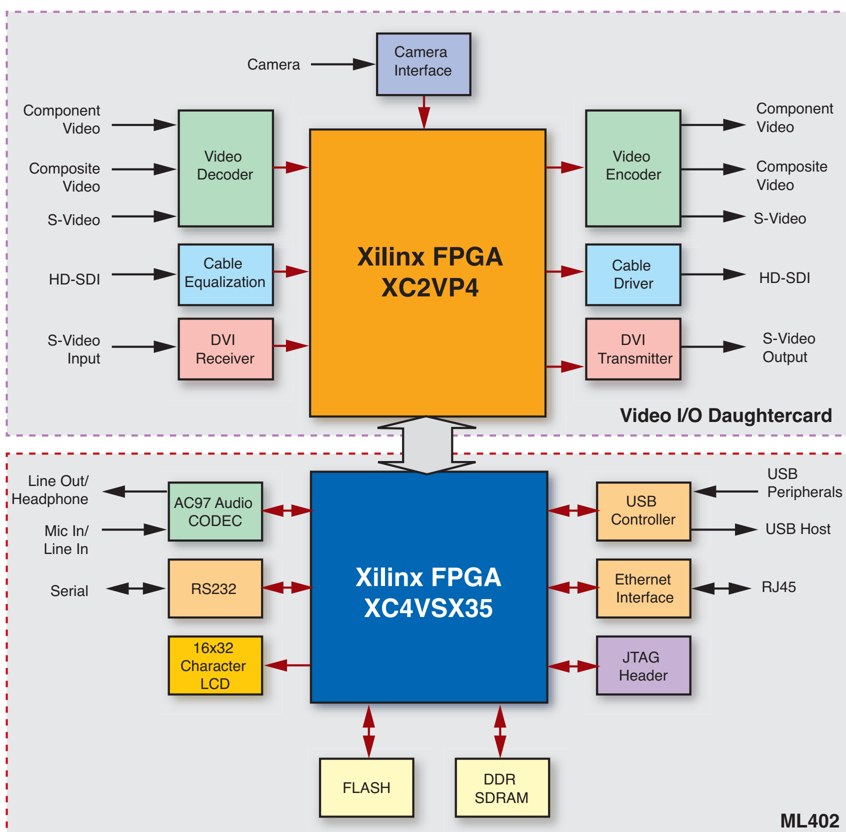

Figure 2 - Block diagram of Video Starter Kit 4VSX35

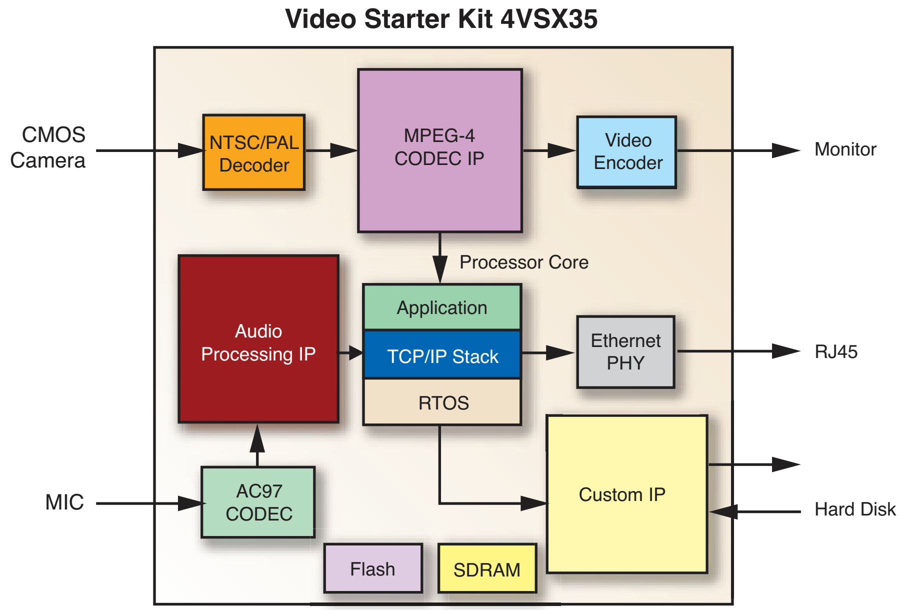

Figure 3 - Network surveillance camera

from the VSK to the PC, another innovative high-speed hardware co-simulation through an Ethernet interface was introduced in System Generator for DSP 8.1. This interface allows high throughput with low latency, which proved to be extremely useful when building video/imaging systems in the System Generator environment.

Network Surveillance Camera Application

FPGAs have historically been found in high-end professional broadcast systems and medical imaging equipment. Today FPGAs are also finding their way into high-volume products such as digital video recorders and network surveillance cameras because of their flexibility in handling a broad range of media formats such as MPEG-2, MPEG-4, H.264, and Windows Media. Their extremely high-performance DSP horsepower also makes FPGAs suitable for other challenging video and audio tasks.

Typically, a network surveillance camera product comprises three parts: a camera to convert the real-world image into a video stream; a video decoder for streams compressed into H.264, MPEG-2, or another format; and a video/image processor for de-interlacing, scaling, and noise reduction before packeting the digitized video for transmission over the Internet.

FPGAs can have many areas of responsibility within surveillance cameras, as shown in Figure 3. Bridging between standard chipsets as "glue logic" has always been a strong application of FPGAs, but many more image-processing tasks (such as color-space conversion), IDE (Integrated Drive Electronics) interface, and support for network interfaces (such as IEEE 1394) are now also commonly implemented in low-cost programmable devices.

With high-performance DSP capability inside a network surveillance camera, you can digitize and encode the video stream to be sent over any computer network. You can use a standard Web browser to view live, full-motion video from anywhere on a computer network, including over the Internet. Installation is simplified by using existing LAN wiring or wireless LAN. Features such as intelligent video, e-mail notification, FTP uploads, and local hard-disk storage provide enhanced differentiation and superior capability over analog systems.

The hard-processor core is an IBM PowerPC 405 immersed in a Xilinx Virtex™-II Pro™ FPGA, delivering 600 DMIPS at 400 MHz running MontaVista Linux or Wind River Systems's VxWorks real-time operating system (RTOS), as well as a network protocol stack to implement these features.

Xilinx also offers the MicroBlaze™ 32-bit RISC processor core, delivering up to 138 DMIPS at 150 MHz and 166 DMIPS at 180 MHz when used in the Virtex-II Pro and Virtex-4 devices, respectively.

Conclusion

Bandwidth is precious; to make the most of it, compression schemes have steadily improved – and new algorithms push the envelope even further. As such, system-processing rates have increased over time, and real-time image processing is an ideal way to meet these requirements while removing memory overhead.

At the same time, Moore's Law has resulted in low-cost programmable logic devices, such as the new FPGAs, that provide the same functionality and performance previously found only in expensive professional broadcast products.

FPGAs provide both professional and consumer digital broadcast OEMs with real-time image processing capabilities that address the system requirements of new and emerging video applications. Compared to other technologies, FPGAs offer an unrivalled flexibility that enables you to get your products to market quickly. Remote field upgradeability means that systems can be shipped now and features, upgrades, or design fixes added later.

The VSK has been architected to reduce implementation risks, time to market, and development costs. By providing hardware and MPEG-4 IP in a pre-tested and integrated platform, you can concentrate on implementing the application-specific video and imaging functionality that is most relevant to your particular product.

For more information, visit *www.xilinx.com/products/design_resources/dsp_central/grouping/index.htm.*