

Course Description

The DSP Design Flow course provides the advanced tools and expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, as well as HDL design flow, CORE Generator™ software, design implementation tools, and hardware-in-the-loop verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

Level – Intermediate

Course Duration – 3 days

Price – \$1500 USD or 15 Training Credits

Course Part Number – DSP10000-7-ILT

Who Should Attend? – System engineers/designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using MathWorks MATLAB and Simulink and using Xilinx System Generator for DSP

Prerequisites

- Fundamentals of MATLAB/Simulink and Xilinx FPGAs
- Basics of digital signal processing theory for functions, such as FIR (Finite Impulse Response) filters, oscillators and mixers, and FFT (Fast Fourier Transform) algorithms

Software Tools

- ISE™ 7.1i SP3
- System Generator for DSP
- EDK 7.1i SP2
- ChipScope™ Pro 7.1.3
- Mentor Graphics ModelSim
- The MathWorks MATLAB

After completing this comprehensive training, you will have the necessary skills to:

- Describe the different design flows for implementing DSP functions, with a large focus on System Generator
- Identify Xilinx FPGA capabilities and know how to implement a design from algorithm concept to hardware simulation
- Implement a design from start to finish by using System Generator
- Perform hardware-in-the-loop and HDL co-simulations and improve productivity
- Integrate the ChipScope™ Pro block in a design and analyze the design
- Develop a hardware co-simulation model using System Generator Board Description Builder
- Integrate a System Generator design as a peripheral in a MicroBlaze™ processor-based system

Course Outline

Note: Target architectures include Virtex™-4, Virtex-II Pro, and Spartan™-3E FPGAs.

Day 1: DSP Design Implementation Tools

- Introduction
- DSP Design Flows in FPGAs
- **Lab 1:** Creating a 12 x 8 MAC Using VHDL
- **Lab 2:** Creating a 12 x 8 MAC Using the Xilinx Architecture Wizard
- **Lab 3:** Creating a 12 x 8 MAC Using the Xilinx System Generator

Day 2: Digital Signal Processing Functions

- Digital Filtering
- **Lab 4:** Designing a FIR Filter
- HDL Co-Simulation
- **Lab 5:** MAC FIR Filter Verification Using Simultaneous Co-Simulations
- Looking Under the Hood
- **Lab 6:** Looking Under the Hood
- Controlling the System
- **Lab 7:** Controlling the System

Day 3: Digital Signal Processing Functions

- Multi-Rate Systems
- **Lab 8:** Designing a MAC-Based FIR Using the DSP48 Slice
- Advanced Features
- **Lab 9:** Designing Using the PicoBlaze Microcontroller
- **Lab 10:** Creating Parametric Designs
- **Lab 11:** Integrating the ChipScope Pro Analyzer
- **Lab 12:** A System Generator Design as an XPS Peripheral

Lab Descriptions

This lab-intensive class gives you hands-on experience by using System Generator for DSP to visualize, simulate, verify, and implement DSP algorithms in Xilinx FPGAs. The labs start at a descriptive level and build on each other. You should expect each successive lesson's challenges to increase. In addition, the labs included in the Advanced Features module provide you experience with other tools such as the ChipScope Pro analyzer and the Embedded Development Kit. System Generator for DSP 7.1 features are identified, including hardware and software co-simulation verification.

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and training credits.

Course Description

This course shows you how to take advantage of the features available in the Xilinx FPGA architecture, including the Virtex™-4 FPGA, and describes how DSP algorithms can be implemented efficiently. The techniques also demonstrate which decisions at the system level have the greatest impact on the implementation process and product costs.

Level – Advanced

Course Duration – 3 days

Price – \$1800 USD or 18 Training Credits

Course Part Number – DSP20000-7-ILT

Who Should Attend? – Engineers and designers who have an interest in developing products that use digital signal processing

Prerequisites

A fundamental understanding of digital signal processing theory, including an understanding of the following principles:

- Sample rates
- Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters
- Oscillators and mixers
- Fast Fourier Transform (FFT) algorithm

After completing this comprehensive training, you will have the necessary skills to:

- Describe how DSP algorithms can be implemented efficiently by using Xilinx FPGA technology
- Identify the capabilities and features of the various Xilinx FPGA families to implement efficient DSP algorithms
- Establish methods for the accurate estimation of silicon area consumption and cost
- Evaluate which algorithms are best suited for FPGA implementation and identify which algorithms are less desirable
- Assess how system-level decisions impact hardware implementation and how hardware implementation can enhance results at the system level

Course Outline

Day 1

- On the Same Wavelength
 - Basic terminology and acronyms used in DSP design
 - Sample rates and bit widths used in DSP applications
 - DSP building blocks and processing requirements
- Some Bits About Numbers
 - Numbering formats, range, and precision
 - Mathematical operations using a variety of formats
- Tuning the Receiver
 - Structure and Resources of Xilinx Devices
 - Estimating DSP building block sizes

Day 2

- Tuning the Receiver (continued)
 - Implementing the multiplication function
 - Bit-width impact on system-level decisions
- Memories are Made of This
 - Block versus distributed memory
 - SRL16E and the delay function
 - Memory aspect ratios and their manipulation
- Selective Filters
 - FIR filter specifications and implementation
 - Selecting a technique for a given specification
 - Effects of halfband and interpolated filters

Day 3

- One Filter Does Not Make a System
 - Options to be considered with multiple channels
 - Interpolation and decimation
 - Rate changing and its effect on FIR filter choice
 - Filtering algorithms that exploit device architecture
 - Importance of connectivity versus isolated functions
- Do Not Block the Datapath
 - Numeric controlled oscillators and mixers
 - Strategies for FFT implementation
 - Achieving bandwidth requirements of the FFT
 - Using the FPGA as an efficient co-processor

Course Exercises

- MAC Rates and Memory Requirements
- Constructing a 128-Tap FIR Filter
- Fractional Number Formats
- Twos Complement Arithmetic
- Summation by Addition Tree
- Summation by Addition Chain
- Full Adder: How Many Slices?
- Summation Structure Sizes
- Serial Summation Structure
- 8-Bit by 12-Bit Multiplier
- KCM Multipliers
- Distributed RAM for FIFO
- Size Estimates for Delay Structures
- Using the SRL16E as a FIFO
- Creating Larger RAM Structures
- Selecting a MAC FIR Technique
- Parallel FIR Filter Size
- Symmetry, Interpolation, and Phases
- Decimation Filter
- “fs/4” Mixing and Decimation
- Designing a Numeric Controlled Oscillator (NCO)
- FFT: Benchmarks and Transform Time
- Collection Time = Processing Time
- 128-Point FFT in 1.28 μ s

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