

Accelerate Video DSP Co-Processing Designs

Design, develop, and test your algorithms with the Video Virtual Socket Adapter.

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Did you know that you can evaluate, test, develop, and benchmark custom video processing applications utilizing an appropriate mixture of FPGA and DSP processing? The new Xilinx® Video Virtual Socket Adapter (VSA) is designed to accelerate FPGA/DSP video co-processing development.

The VSA is a plug-and-play system comprising a Spectrum Digital DM642 EVM DSP evaluation board; a Spectrum Digital XEVM642 daughtercard; a VHDL “virtual socket” framework for the Virtex™-4 SX FPGA; DSP firmware; a System Generator for DSP demo module featuring a two-dimensional 5 x 5 Video FIR filter; user guide; application notes; and a PC-based network streaming MJPEG video player. With the bundled demo system, you instantly get the infrastructure to rapidly prototype your video applications to accelerate FPGA/DSP co-processing product development. The system was developed by Nuvation, a Xilinx Alliance Program design services firm, and is being distributed by Xilinx.

The VSA System

Figure 1 shows a block diagram of the VSA system. Spectrum Digital's DM642 EVM showcases TI's DM642 digital media processor (TMS320DM642). On-board components include 32 MB SDRAM, 4 MB Linear Flash, two video decoders, one video encoder, two S-Video/composite video inputs, one S-Video/composite/VGA output, 10/100 Ethernet PHY, mic and headphone jacks, and an off-board connector driven through the DM642's EMIF interface. You can develop DSP firmware on the DM642 EVM with TI's Code Composer Studio and a JTAG emulator.

XEVM642 Virtex-4 Daughtercard

Spectrum Digital's XEVM642 is a Virtex-4 SX35-based daughtercard that plugs into the DM642 EVM. In addition to the Virtex-4 device, the XEVM has memory, clocks, a JTAG port, and a Compact Flash card socket. From video algorithm acceleration, data compression filters, and custom logic, the Virtex-4 FPGA is easily programmable with Xilinx System Generator for DSP and ISE™ software.

VHDL and Firmware

The Video VSA includes a set of VHDL modules and the firmware to directly control them (illustrated in Figure 2). These modules include a generic user logic module (the function that fits into the "virtual socket"), a video input module, a test pattern generator, a 2:1 video switch, a video output module, and a host interface module. All of these modules – and the firmware that controls them – are reusable.

The Video VSA modules are connected together in a way that provides a "virtual socket" where the user function can reside. Any appropriate functionality and implementation approach of the user function is possible; the surrounding Video VSA modules are connected together to form the infrastructure that allows you to focus your design effort on the user function.

The demo firmware comprises four main components, shown in Figure 3 as shaded blocks within the overall demo firmware framework.

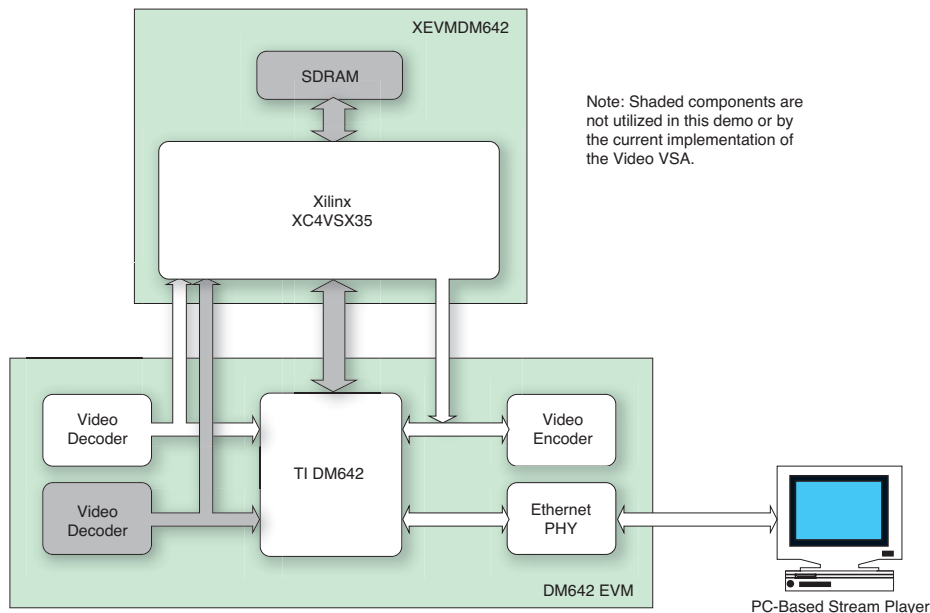


Figure 1 – Block diagram of EVM642 and XEVM system

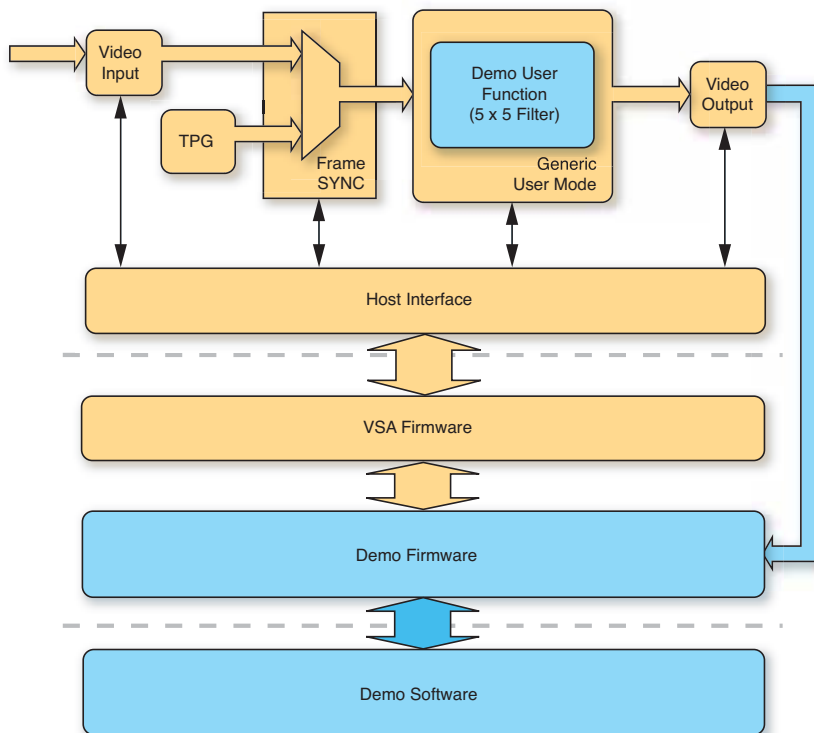


Figure 2 – Video VSA system block diagram

Video Conversion Pipeline

This component comprises two independently running pipelined tasks. The first receives a video stream from the FPGA video output port through a DM642 video input port and converts it to YUV420 format. The second compresses it into an in-memory JPEG image for use by the MJPEG

player server and HTTP server components. It passes new frames to the MJPEG player server when they are available.

MJPEG Player Server

This task awaits incoming connections from the PC-based MJPEG player client and streams out newly captured JPEG

images while the connection is active. This task receives notification from the video conversion pipeline when a new JPEG image is available.

Demo Control

The demo control component is a task that polls the video's locked status and video standard for changes. This task will re-initialize the video conversion pipeline when video lock has been restored. It is also used to handle 525/625 video standard changes.

During the same polling loop, the demo's processing window position is updated (if movement is enabled). This implements the window's bouncing behavior.

The remainder of the demo control component is a series of demo-specific functions responsible for controlling the following demo settings:

- Processing window position, size, enabled status, and auto move
- Filter kernel (including chroma bypass)
- Video source selection (test pattern or live video)

Web Server

The Web server is configured to use a standard HTTP port and offers the following content/services:

- The current video frame is made available as a JPEG file
- A JavaScript-based player/control console for the demo is available as the default web page on the server; this page also loads two static logo images from the Web server
- Three dynamic CGI scripts process incoming HTTP POST configuration change requests used by both the MJPEG player and the default Web-based player to control the demo
- A dynamic website for running automated tests on the host interface

VSA Demo Application

The system includes a filter application that demonstrates one of many possible functions that you can implement in the VSA. The function is a two-dimensional 5 x 5 FIR filter with a configurable rectangular window

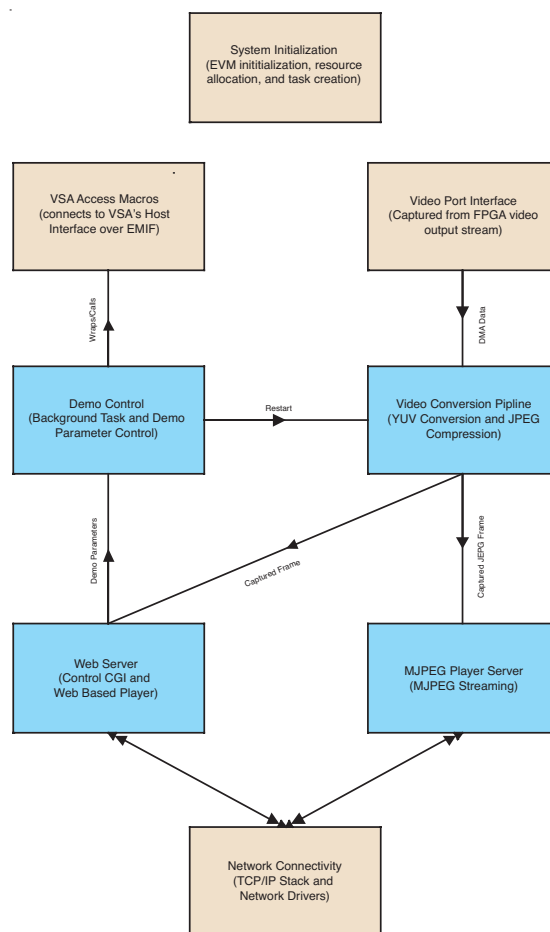


Figure 3 – VSA firmware component overview



Figure 4 – MJPEG player (showing live video with edge-detect function)

that filters video samples within the processing window while passing all other samples unmodified. The position and size of the processing window is implemented to allow uninterrupted video streaming during modification. Figure 4 shows a snapshot of a live streaming video display featuring an edge detect filter kernel.

The filter coefficients are represented in 16-bit signed 2's complement fixed-point format, allowing implementations of high-precision video filters with gain. The coefficients are loadable at runtime and are designed to engage without disturbing the video stream. The resulting video is normalized and clamped in accordance with ITU-R BT.656/601 as a post-processing step in the filter.

The filter is fully implemented in a Xilinx System Generator for DSP workflow that operates under The MathWorks's Simulink environment. System Generator for DSP provides abstractions that enable you to develop highly parallel systems in Xilinx FPGAs, providing system modeling and automatic code generation from Simulink and MATLAB, also from The MathWorks.

The purpose of the Video VSA demo is to showcase the process to customize Video VSA modules for your application. A detailed application note is included with the package, along with a demo user guide to facilitate a quick start to your development.

Conclusion

The new Video Virtual Socket Adapter from Xilinx enables rapid algorithm porting and verification for video system development, utilizing Xilinx Virtex-4 SX platform devices and TI DM642 digital media processor DSPs in the System Generator for DSP tool flow. The VSA hardware and associated TI DSP tools are available from Spectrum Digital (www.spectrumdigital.com). For all other VSA inquiries, please contact your local Xilinx representative or visit www.nuvation.com.