

### Course Description

The DSP Design Flow course provides the advanced tools and expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, HDL co-simulation, and hardware-in-the-loop verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

**Level** – Intermediate

**Course Duration** – 3 days

**Price** – \$1500 USD or 15 Training Credits

**Course Part Number** – DSP10000-8-ILT

**Who Should Attend?** – System engineers/designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using MathWorks MATLAB and Simulink and using Xilinx System Generator for DSP

#### Prerequisites

- Fundamentals of MATLAB/Simulink and Xilinx FPGAs
- Basics of digital signal processing theory for functions, such as FIR (Finite Impulse Response) filters, oscillators and mixers, and FFT (Fast Fourier Transform) algorithms

#### Software Tools

- ISE™ 8.1i
- System Generator for DSP 8.1
- EDK 8.1
- ISIM Simulator 8.1
- ChipScope™ 8.1
- Mentor Graphics ModelSim PE 6.0c
- MATLAB with Simulink R14 SP1

After completing this comprehensive training, you will have the necessary skills to:

- Describe the different design flows for implementing DSP functions, with a large focus on System Generator
- Identify Xilinx FPGA capabilities and know how to implement a design from algorithm concept to hardware simulation
- Implement a design from start to finish by using System Generator
- Perform hardware-in-the-loop and HDL co-simulations and improve productivity
- Integrate the ChipScope Pro block in a design and analyze the design
- Develop a hardware co-simulation model using System Generator Board Description Builder
- Integrate a System Generator design as a peripheral in a MicroBlaze™ processor-based system
- Utilize timing analyzer block to improve design performance

### Course Outline

**Note:** Target architectures include Virtex™-4, Virtex-II Pro, and Spartan™-3E FPGAs.

#### Day 1

- Introduction
- DSP Design Flows in FPGAs
- **Lab 1:** Creating a 12 x 8 MAC Using the Xilinx System Generator
- Digital Filtering

- **Lab 2:** Designing a FIR Filter
- HDL Co-Simulation
- **Lab 3:** MAC FIR Filter Verification Using Simultaneous Co-Simulations

#### Day 2

- Looking Under the Hood
- **Lab 4:** Looking Under the Hood
- Controlling the System
- **Lab 5:** Controlling the System
- Multirate Systems
- **Lab 6:** Designing a MAC-Based FIR Using the DSP48 Slice

#### Day 3

- Advanced Features
- **Lab 7:** Integrating the ChipScope Pro Analyzer
- **Lab 8:** A System Generator Design as an XPS Peripheral
- **Lab 9:** Multiple Clock Domains Design Using Shared Memories
- **Lab 10:** Improving Design Performance Using Timing Analyzer
- **Lab 11:** Designing Using the PicoBlaze™ MicroController
- **Lab 12:** Creating Parametric Designs

### Lab Descriptions

This lab-intensive class gives you hands-on experience by using System Generator for DSP to visualize, simulate, verify, and implement DSP algorithms in Xilinx FPGAs. The labs start at a descriptive level and build on each other. You should expect each successive lesson's challenges to increase. In addition, the labs included in the Advanced Features module provide you experience with other tools such as the ChipScope Pro analyzer and the Embedded Development Kit. System Generator for DSP 8.1 features are identified, including hardware and software co-simulation verification.

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