

Leveraging the Virtex-5 SXT High-Performance DSP Solution

The SXT platform maximizes DSP bandwidth and minimizes power consumption.

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For more than 20 years FPGAs have provided the most flexible, adaptive, rapid design environment available. Early on, DSP designers discovered that a reprogrammable sea of gates could be used for digital signal processing. By combining multipliers, adders, and accumulation units built into the FPGA fabric, you could leverage massive parallelism to implement efficient DSP filter algorithms.

What was sacrificed in raw frequency performance was more than made up for in parallelism, achieving DSP bandwidth comparable to alternative solutions. Over time, multiplier and adder implementations became more efficient, and in 1998 Xilinx introduced the first embedded multiplier integrated within the Virtex™-II FPGA family. Wildly popular, the Xilinx® Virtex-II and Virtex-II Pro families took FPGA-based DSP to a new level, breaking the billion MAC operations-per-second barrier.

Fueled by demand in the digital communication, military, defense, and video and imaging markets, Xilinx made addi-

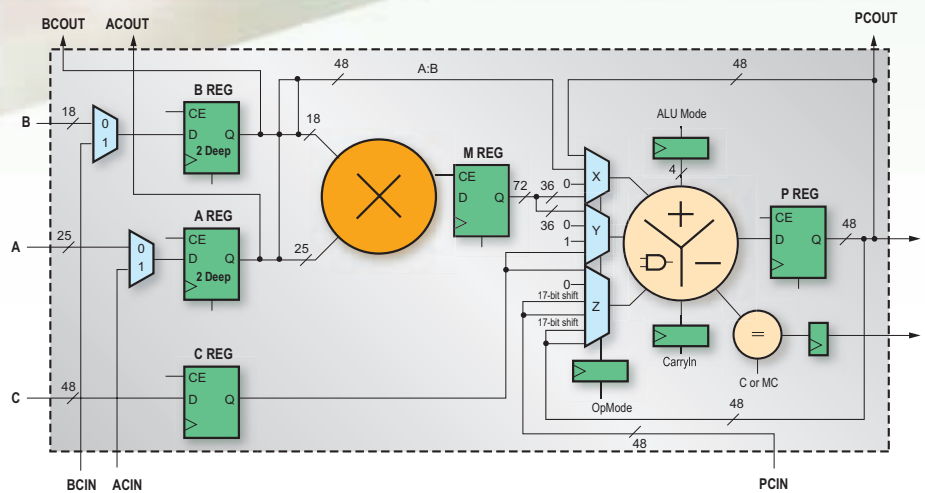


Figure 1 – Diagram of the DSP48E slice in Virtex-5 FPGAs

tional changes to address unique challenges and augment the massively parallel implementation style. As performance and the number of multipliers and adders increased, managing power consumption became more difficult.

Xilinx engineers found a solution to this challenge by designing the DSP48 slice, an ultra-low-power, high-performance, comprehensive digital signal processing element that could be cascaded easily without using any FPGA fabric resources. This element was further enhanced in Virtex-5 devices; the renamed DSP48E slice supports higher

precision, SIMD (single instruction, multiple data) operation, integrated pattern detect circuitry, and a logic unit.

The demand for fast on-chip data and coefficient storage prompted Xilinx to architect a digital signal processing platform that included a unique ratio of DSP48E slices and an abundance of block RAM and distributed RAM. Finally, to move data in and out of the chip faster, Xilinx included integrated high-speed serial channels running as fast as 3.125 Gbps. The combination of these elements is the Virtex-5 SXT platform.

The Virtex-5 SXT Engine – The DSP48E Slice

Understanding the evolution in digital signal processing within an FPGA must include a review of the DSP48E slice (see Figure 1), and the three main aspects of its design:

- Integrated multiplier and second stage. Expanding the multiplier operation with an integrated second-stage adder/subtractor/accumulator. You can now implement the most common combination of DSP operations within a single DSP48E slice.
- Systolic implementation. To increase performance and minimize power consumption, DSP48E slices are self-contained elements designed to interface together like building blocks, each containing dedicated routing and buffering independent of the FPGA fabric.
- Fully custom design. Xilinx determined early on that to reach advanced levels of performance and achieve very low power consumption, a full custom design tailored to the latest process geometry would be necessary. Xilinx design teams worked with Arithmetica, integrating MathIP libraries for the multiplier and adder circuitry to further increase efficiency.

With this design, the implementation of the DSP48E slice achieves unprecedented levels of performance and low power efficiency. The DSP48E slice in Virtex-5 devices runs at 550 MHz, 500 MHz, and 450 MHz in the fastest, mid-, and slowest speed grades, respectively. This performance is possible whether you are using one DSP48E slice by itself or combining all 640 DSP48E slices within the largest Virtex-5 SXT device (using the dedicated cascade logic to achieve 352 billion multiply accumulate operations per second). This truly amazing performance is achieved using only the DSP48E slices and consumes no logic or FPGA routing resources.

This dedicated cascade logic means that power consumption is calculated based on each DSP48E slice, the speed at which it runs, and the toggle rate of the inputs. Measured typical power consumption of an individual DSP48E slice is 1.38 mW/100 MHz. You can easily calculate that the total

dynamic power consumption of DSP48E slices – running all 640 slices in a Virtex-5 SX95T device at 550 MHz with a typical 38% toggle rate – is 4.92W.

Low-Power, High-Performance Design Techniques

To take full advantage of the unique Virtex-5 SXT architecture for digital signal processing, I recommend following these simple guidelines:

- Implement filter algorithms that maximize DSP48E slice usage. Each 25 x 18-bit DSP48E slice is equivalent to more than 500 slices of programmable logic, consumes 1/10 the power of an equivalent logic implementation, and runs as fast as 550 MHz alone or chained together.
- Take advantage of all DSP48E slice capabilities. Each DSP48E slice can be configured as a stand-alone 25 x 18 multiplier, a 25 x 18-bit multiplier plus adder/subtractor/accumulator, or as a 48 x 48-bit adder or subtractor. Each DSP48E slice supports SIMD operations and symmetric or convergent rounding.
- Implement fixed-point or floating-point operations. Not only is the DSP48E slice ideal for fixed-point FIR, FFT, or complex filter operations, the 25 x 18 input size and cascade routing enable efficient 24 x 24 unsigned floating operations using two DSP48E slices.

Applying the DSP48E Slice in a Digital Signal Application

The unique combination of DSP48E slices, block RAM, logic, and multi-gigabit transceivers in the Virtex-5 SXT platform provides a cost-effective, high-performance,

low-power solution for DSP filter applications. To illustrate this, let's look at a wireless radio card application implemented in both the Virtex-4 SX and Virtex-5 SXT device platforms, comparing power consumption for both implementations.

The WiMAX digital front end (DFE) integrates the following components: digital up conversion (DUC)/digital down conversion (DDC), crest factor reduction (CFR), and automatic gain control (AGC). The filtering required in this design is a perfect match for the DSP48E slices available in either a Virtex-4 SX25 FPGA or a Virtex-5 SX35T FPGA. The design runs at 276 MHz and consumes 73% of the DSP48 resources in the Virtex-4 SX25 FPGA (95 out of 128) or 48% of the DSP48E resources in the Virtex-5 SX35T FPGA (95 out of 196).

Although the performance and resources used to implement the WiMAX DFE solution are amazing alone, it is the power efficiency that is truly remarkable. This design primarily uses either DSP48 or DSP48E slices but also consumes block RAM and logic. Table 1 compares these solutions and shows the measured power consumption and reduction going from Virtex-4 devices to Virtex-5 devices.

Conclusion

As digital signal processing requirements grow and the challenge to provide scalable high-performance DSP increases, so will the challenge to manage power consumption at levels hundreds of GMACs per second and higher. The Xilinx Virtex-5 SXT FPGA platform provides a unique single-chip solution that leverages massive parallelism to achieve ultra-high performance while minimizing power consumption. For more information on Xilinx DSP solutions, visit www.xilinx.com/dsp.

Design	Virtex-4 Power (W)	Virtex-5 Power (W)	Percent Decrease
DUC + CFR	0.858	0.552	35.6
DDC + AGC	0.740	0.478	35.4
Total DFE	1.598	1.030	35.5

Table 1 – Measured power consumption in a real-world application