



DSP Application Notes

Jumpstart your DSP design with Xilinx application notes describing specific design examples and methodologies.

Wireless Solutions

PN Generators Using the SRL Macro	XAPP211	www.xilinx.com/bvdocs/appnotes/xapp211.pdf
Hardware Acceleration of 3GPP Turbo Encoder/Decoder BER Measurement Using System Generator	XAPP948	www.xilinx.com/bvdocs/appnotes/xapp948.pdf
PowerPC Processor with Floating Point Unit for Virtex-4 FX Devices	XAPP547	www.xilinx.com/bvdocs/appnotes/xapp547.pdf
Continuously Variable Fractional Rate Decimator	XAPP936	www.xilinx.com/bvdocs/appnotes/xapp936.pdf

Multimedia, Video, and Imaging Solutions

Color-Space Converter: RGB to YCrCb	XAPP930	www.xilinx.com/bvdocs/appnotes/xapp930.pdf
Color-Space Converter: YCrCb to RGB	XAPP931	www.xilinx.com/bvdocs/appnotes/xapp931.pdf
Chroma Resampler	XAPP932	www.xilinx.com/bvdocs/appnotes/xapp932.pdf
Two-Dimensional Linear Filtering (2D FIR)	XAPP933	www.xilinx.com/bvdocs/appnotes/xapp933.pdf
Video Virtual Socket Architecture Demo System	XAPP919	www.xilinx.com/bvdocs/appnotes/xapp919.pdf

Defense Systems Solutions

High-Speed DES and Triple DES Encryptor/Decryptor	XAPP270	www.xilinx.com/bvdocs/appnotes/xapp270.pdf
QDR II SRAM Interface for Virtex-5 Devices	XAPP853	www.xilinx.com/bvdocs/appnotes/xapp853.pdf
RLDRAM II Memory Interface for Virtex-5 FPGAs	XAPP852	www.xilinx.com/bvdocs/appnotes/xapp852.pdf

Design Methodology

PowerPC Processor with Floating Point Unit for Virtex-4 FX Devices	XAPP547	www.xilinx.com/bvdocs/appnotes/xapp547.pdf
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Error Correction

Viterbi Decoder Block Decoding - Trellis Termination and Tail Biting	XAPP551	www.xilinx.com/bvdocs/appnotes/xapp551.pdf
Multiple Bit Error Correction	XAPP715	www.xilinx.com/bvdocs/appnotes/xapp715.pdf
Hardware Acceleration of 3GPP Turbo Encoder/Decoder BER Measurement Using System Generator	XAPP948	www.xilinx.com/bvdocs/appnotes/xapp948.pdf

DSP Processor Interfaces

Alpha Blending Two Data Streams Using a DSP48 DDR Technique	XAPP706	www.xilinx.com/bvdocs/appnotes/xapp706.pdf
Interfacing Virtex-II FPGAs With Analog Devices TigerSHARC TS20x DSPs via LVDS Link Ports	XAPP635	www.xilinx.com/bvdocs/appnotes/xapp635.pdf
Interfacing Xilinx FPGAs to TI DSP Platforms Using the EMIF	XAPP753	www.xilinx.com/bvdocs/appnotes/xapp753.pdf
Video Virtual Socket Architecture Demo System	XAPP919	www.xilinx.com/bvdocs/appnotes/xapp919.pdf

Transform

Video Compression Using DCT	XAPP610	www.xilinx.com/bvdocs/appnotes/xapp610.pdf
Video Compression Using IDCT	XAPP611	www.xilinx.com/bvdocs/appnotes/xapp611.pdf

FPGA Devices

DDR SDRAM Controller Using Virtex-5 FPGAs	XAPP851	www.xilinx.com/bvdocs/appnotes/xapp851.pdf
RLDRAM II Memory Interface for Virtex-5 FPGAs	XAPP852	www.xilinx.com/bvdocs/appnotes/xapp852.pdf
QDR II SRAM Interface for Virtex-5 Devices	XAPP853	www.xilinx.com/bvdocs/appnotes/xapp853.pdf
16-Channel, DDR LVDS Interface with Per-Channel Alignment	XAPP855	www.xilinx.com/bvdocs/appnotes/xapp855.pdf
SFI-4.1 16-Channel SDR Interface with Bus Alignment	XAPP856	www.xilinx.com/bvdocs/appnotes/xapp856.pdf
High-Performance DDR2 SDRAM Interface in Virtex-5 Devices	XAPP858	www.xilinx.com/bvdocs/appnotes/xapp858.pdf
16-Channel, DDR LVDS Interface with Real-Time Window Monitoring	XAPP860	www.xilinx.com/bvdocs/appnotes/xapp860.pdf
Efficient 8X Oversampling Asynchronous Serial Data Recovery Using IDELAY	XAPP861	www.xilinx.com/bvdocs/appnotes/xapp861.pdf
Configuring Xilinx FPGAs with SPI Serial Flash	XAPP951	www.xilinx.com/bvdocs/appnotes/xapp951.pdf