

Embedded Application Notes

Popular application notes available from Xilinx and our partners.

In this section, we'll break out excerpts from Xilinx® application notes and provide information on how to access the complete articles. The first two application notes are “High Performance TCP/IP on Xilinx FPGA Devices Using the Treck Embedded TCP/IP Stack,” by Satish Narayanaswamy of Xilinx (XAPP546) and “UltraController-II: Minimal Footprint Embedded Processing Engine” by Punit Kalra, also from Xilinx (XAPP575).

XAPP546 describes how to use the Treck TCP/IP stack with Xilinx EDK tools and the Gigabit System Reference Design (GSRD) system.

XAPP575 presents the features and benefits of the PowerPC™-based UltraController-II, along with a tutorial of applications included with the design.

XAPP546: High Performance TCP/IP on Xilinx FPGA Devices Using the Treck Embedded TCP/IP Stack

TCP/IP is a popular communications protocol software stack that allows reliable data communications between two hosts. Most people already use TCP/IP to check e-mail, browse the Web, or transfer files. TCP/IP is being used more and more in the embedded world as well.

Treck, Inc. is a leading provider of embedded TCP/IP stacks that allow Xilinx FPGAs to communicate in a wide range of networking environments. Treck's dual Ipv4/Ipv6 TCP/IP stack provides Ipv4 functionality today and allows a Xilinx FPGA to support Ipv6 networks of the future. Treck also provides optional protocols, such as an embedded web server, FTP, IPSEC, and DHCP, to enhance the functionality of Xilinx FPGAs.

This application note describes how to get started using the Treck TCP/IP stack



using Xilinx EDK tools. An evaluation version of the Treck TCP/IP stack is included. An example TCP application uses the Treck TCP/IP stack to send TCP data over Gigabit Ethernet on the Virtex™-II Pro ML300 development board to a remote PC-based server.

Introduction

The Treck TCP/IP stack offers a high-performance TCP/IP software solution that can be used with the PowerPC™ 405 processor inside the Virtex-II Pro series of Xilinx FPGAs.

Some features of the Treck TCP/IP stack include:

- Zero-copy send and receive, which help deliver maximum throughput for bridging applications
- Jumbo frames support (in the case of Gigabit Ethernet devices)
- TCP checksum offload support for devices that support TCP checksum offload in hardware

- Fully RFC-compliant TCP/IP stack for maximum interoperability
- Standard sockets interface API

The Treck TCP/IP stack can be used with or without any operating system software. This application note discusses the use of the Treck TCP/IP stack on a stand-alone system (without an operating system).

This application note also provides the Treck library as a binary file for evaluation purposes. The Treck library allows full functionality of the stack for a limited period of time before it times out and requires a restart to continue evaluation.

Contact Treck at www.treck.com for information about purchasing the sources for the Treck TCP/IP stack. An example TCP client and server application is also available as part of this application note. Xilinx EDK tools are used to compile and link the client application with the Treck library to create a complete TCP/IP application for the ML300 board.

The client application uses Treck TCP/IP on the ML300 board to transmit TCP data to a remote PC. The server application running on the PC prints the TCP throughput every second on the console. The sources, as well as Windows and Linux binaries, are included for the server application.

The reference design files can be downloaded from the Xilinx website.

The Treck embedded TCP/IP stack is well suited for TCP/IP applications running on Xilinx FPGAs. Its support of zero-copy applications and checksum offload in hardware is utilized in a high-performance architecture like GSRD. Treck also offers different protocols and applications like IPSEC, IPV6, HTTP, and Telnet. The combination of the Treck TCP/IP stack and the flexible Xilinx FPGA hardware

platform offers an ideal solution for TCP/IP termination at high data rates.

For more of XAPP546, you can access the unabridged application note for “High Performance TCP/IP on Xilinx FPGA Devices Using the Treck Embedded TCP/IP Stack” at www.xilinx.com/bvdocs/appnotes/xapp546.pdf.

XAPP575: UltraController-II: Minimal Footprint Embedded Processing Engine

UltraController-II is a minimal footprint Virtex-II Pro embedded processing engine based on the embedded PowerPC 405 (PPC405) processor core. Computing performance is maximized and FPGA resource usage minimized by running code strictly from the integrated PPC405 caches. General-purpose input/output (GPIO) is available directly from the PPC405 core. Interrupt handling is provided for a user-defined external interrupt line, a programmable interval timer (PIT), and a fixed interval timer (FIT). You can easily incorporate the UltraController-II black-box processing engine into larger ISE™ software designs to gain additional degrees of freedom by balancing the high performance of FPGA fabric with the algorithmic flexibility of software.

This application note presents the features and benefits of the UltraController-II, along with a brief overview of the tutorial applications included with the design. The accompanying tutorials and reference designs include VHDL, Verilog, and example C-code applications with step-by-step procedures. XAPP575 also provides performance characteristics and describes how to field an UltraController-II system using Xilinx configuration solutions.

Introduction

The UltraController-II reference design is a black-box processing engine that includes 32 bits of user-defined GPIO as well as interrupt handling capability. UltraController-II applications are developed within the 16 KB instruction- and data-side cache memory of the PPC405 core. If you are developing embedded designs that require PLB and OPB bus resources, the Xilinx Platform Studio (XPS) toolset creates expandable processor designs that leverage the full set of IP and software drivers offered by Xilinx (see www.xilinx.com/ledk).

Features:

- Scalable CPU clock (up to 400 MHz in a Virtex-II Pro speed grade -7 device)
- Integrated cache-based program store
- 16 KB I-side
- 16 KB D-side
- No block RAMs used
- 32-bit output
- 32-bit input
- External user interrupt line (EXT)
- Programmable interval timer (PIT)
- Fixed interval timer (FIT)
- Watchdog timer (WDT)

Benefits:

- Processing power is determined by program execution speed; UltraController-II can be clocked at the maximum PPC405 input clock frequency, which far exceeds any soft-core processor implementation
- Program instruction and data access speeds are maximized by using the integrated caches
- A minimal footprint processing engine frees up FPGA logic and block RAM resources
- 32-bit output and input ports can interface with logic internal or external to the FPGA
- An external interrupt line allows UltraController-II applications to perform high-speed, base-level computation and handle time-critical events as they occur
- Timer resources (PIT and FIT) are available for commonly implemented embedded solutions for:
 - Time-of-day computation
 - Data-logging for system-service routines
 - Periodic servicing of time-sensitive external devices
- A watchdog timer (WDT) is available to monitor system sanity and recover from upsets by issuing a system reset

UltraController-II Internals

In today's complex and competitive design environment, products must be designed and verified more rapidly than ever before. This can be accomplished by partitioning designs into functional sub-blocks. The UltraController-II solution inherently separates a design into hardware and software functional sub-blocks, or components, due to its cache-based nature.

The original block RAM-based UltraController provides you the ability to initialize both the hardware and software components of the system through the bitstream. Compared with traditional embedded systems of similar size, a single bitstream file with both hardware and software components eliminates the need for external non-volatile storage that only contains software.

UltraController-II designs also use a single initialization file. In addition, UltraController-II allows you to independently modify the hardware or software components by taking advantage of Xilinx configuration solutions. You can create multiple software design iterations without modifying the bitstream, thereby limiting the scope of any introduced design changes. Once an UltraController-II black box is integrated into a larger ISE design and verified, the hardware can be locked down to become a “golden” bitstream. This golden bitstream gives you independence from development tool revisions and the ability to reestablish a known hardware state at any time in the future.

UltraController-II offers additional built-in functionality and a reduced resource footprint when compared with UltraController. Program storage for both the instructions and data now resides within the PPC405 caches, thereby eliminating the need for any block RAM. GPIO is available directly from the PPC405 block and provides access to 32 bits of input and output. Exception handling permits you to process a user interrupt line, the PIT, and the FIT interrupts. Reset and boot logic are also covered.

For more of XAPP575, you can access the unabridged application note for “UltraController-II: Minimal Footprint Embedded Processing Engine” at www.xilinx.com/bvdocs/appnotes/xapp546.pdf.