

Tracing MicroBlaze Processors with a Logic Analyzer

Agilent's MicroBlaze trace core and inverse assembler simplify the task.

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Logic analyzers provide deep trace and sophisticated triggering for capturing software trace. These measurements can be critical for tracking events leading up to a crash, evaluating the interaction of software with hardware, or analyzing software performance.

However, microprocessor technology shifts (such as increased use of cache memory) have made the information that can be captured on the pins of stand-alone microprocessors less relevant. These shifts make it increasingly difficult to debug embedded systems. Fortunately, a new logic analysis innovation for Xilinx® FPGAs allows you to quickly take MicroBlaze™ soft-core processor measurements.

Software Execution with Logic Analyzers

Beginning in the 1980s, design teams used logic analyzers extensively to debug embedded systems, designing in PC board connectors with a specified layout for tracing the processor. For 32-bit processors, this requirement typically included 102 to 136 signals comprising data, address, and status signals.

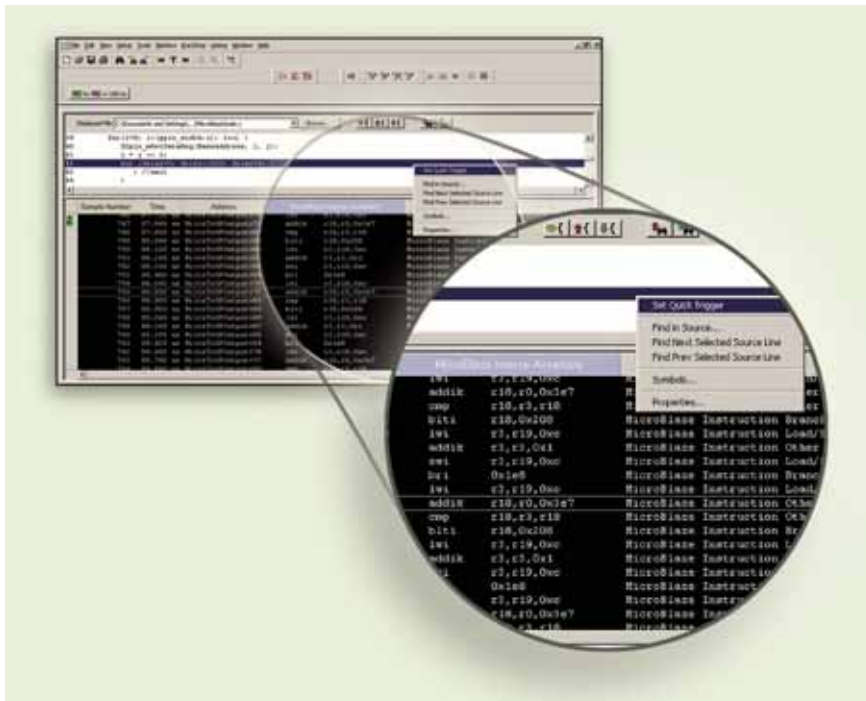


Figure 1 – Agilent's MicroBlaze inverse assembler works with all of Agilent's 1680, 1690, and 16900 series logic. Agilent logic analyzers come standard with a source correlation window so that team members can set up a measurement at the assembly or source level.

Logic analyzers still require a certain arrangement of processor address, status, and data signals to be laid out on your target system. Each processor has an associated logic analysis configuration file and inverse assembler that works with a specified PC board layout. Inverse assembly software converts the acquired ones and zeros to instruction mnemonics.

In the late 1990s, 32-bit embedded processors began incorporating technologies that made it more difficult to make logic analysis trace measurements. Shrinking real estate available for debug made it impractical to include connectors for tracing. Even if the design team had designed in connectors for trace measurement, no signals of relevance would be transmitted to the pins monitored by the logic analyzer if the processor was executing out of cache memory. Turning off cache caused the system to run at a slower rate and could mask problems that would only occur at real system speeds. In addition, pipelining and out-of-order execution made it more difficult for logic analysis vendors to unravel information on the bus.

Recently, Agilent and Xilinx have collaborated to develop a logic analysis trace solution for MicroBlaze processors that overcomes the traditional difficulties of tracing software execution using a logic analyzer.

MicroBlaze Inverse Assembly

For PC board layout, design teams enable the inverse assembler by routing at least the MicroBlaze program counter signals (PC_Ex) and the valid cycle signal (Valid_Instr) to pins. Routing these signals to a specified layout allows for fast connection to a logic analyzer through Mictor, Samtec, or soft-touch probing. You can also connect the logic analyzer to these signals with a berg strip or header, using individual flying leads.

Because of their reprogrammable nature, FPGAs with MicroBlaze processors can be traced late in the development cycle. As long as a sufficient number of pins have been reserved for debug, you can route the required MicroBlaze signals to a specified pinout without PC board changes.

The Agilent inverse assembler for MicroBlaze processors reconstructs program flow by capturing the address of each

executed instruction and looking up the associated opcode in the OMF (object module format) file. It then decodes the opcode into a MicroBlaze mnemonic, as shown in Figure 1.

As pins available for debug are often scarce, the inverse assembler includes a capability that reduces the number of required pins. Although 32 PC_Ex signals exist, the number of external signals needed to capture a logic analysis trace is typically much less. This reduction is accomplished using two different techniques.

First, you do not need to trace the upper address bits. For any given design, a certain number of upper address bits are static. You can achieve more pin reduction – with one additional pin decreased for each static upper address bit in the program counter – by specifying this information in the logic analysis user interface.

Second, you also do not need to trace the lower two address bits. All instructions start on 4-byte boundaries. Using these techniques, tracing software execution of a 1 MB program requires only about 18 pins. Simultaneous capture of data requires additional pins.

Tracing with Cache Enabled and Using Source Correlation

For stand-alone processors with cache enabled, logic analysis tracing becomes impossible. Fortunately, the situation changes for processors embedded in FPGAs. A logic analyzer can trace MicroBlaze processors even when cache is enabled. Captured signals are routed from the execution stage of the MicroBlaze pipeline.

Agilent logic analyzers come standard with a source correlation window. By reading a symbol file (in .elf format), the logic analyzer can associate captured addresses with the high-level software associated with that address. Opcode images are found in the text sections of the .elf object files. As you step through assembly instructions, the equivalent line in the source code for this instruction is also highlighted. You can alternatively step through high-level source code while the logic analyzer simultaneously displays the associated instruction mnemonics in the lower window. Simply

right-click in the source code to set up the logic analysis trigger (trace specification) for the next acquisition, as shown in Figure 1.

MicroBlaze Trace Core (MTC)

An optional MicroBlaze trace core, or MTC, reduces the amount of time and number of pins required to trace MicroBlaze processors with a logic analyzer (see Figure 2). The MTC core, co-developed by Agilent and Xilinx, works exclusively with the Xilinx Platform Studio included with the Embedded Development Kit. Design teams can graphically add an MTC core to their design. Core parameters include pin compression using time-division multiplexing (TDM), pin location, and I/O standards.

The MTC core provides four key values:

1. The MTC core connects required MicroBlaze signals to pins (pre-synthesis).
2. The core incorporates TDM to reduce the number of pins required by a factor of two. Two MicroBlaze signals are TDM'd onto a single pin, with data valid on the rising edge of the clock for signal one and data valid on the falling edge of the clock for signal two. A demux clocking mode in the logic analyzer decompresses the information and splits it into two separate logic analysis channels.
3. The MTC core includes technology that reduces initial setup time from hours to seconds and eliminates manual errors that can happen during PC board layout. Tracing MicroBlaze processors can be accomplished late in product development, as the MTC core eliminates the need to layout a PC

board with a specific MicroBlaze signal pattern for Mictor, Samtec, or soft-touch probes. Through JTAG, the logic analyzer sends an auto setup message to the MTC core. The core outputs a training pattern on a specific MTC pin. The logic analyzer looks for this training pattern across its channels and discovers which channel is connected to the MTC pin. The logic analyzer knows how

each MTC core input is routed through the core to pins from its communication with the MTC core. Using this correlation, the instrument now has sufficient knowledge to determine how to set up the physical connection between specific microprocessor signals and the input channel on the logic analyzer. This process is sequentially repeated for each MTC output pin.

4. Lastly, the MTC core – constructed entirely of flops and LUTs – uses a multi-stage pipeline (typically four) to minimize impact on device timing when the core is inserted (Figure 3). MTC cores are very small. An MTC core in a Xilinx XC2V3000 device consumes roughly 1% of the LUTs and flops.

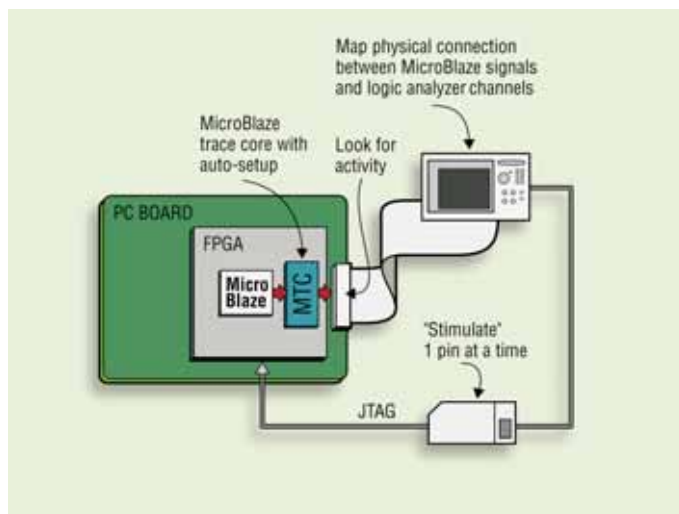


Figure 2 – Agilent's MicroBlaze trace core (MTC) reduces setup time for an initial trace measurement. You can literally connect a logic analyzer to a connector with MTC core outputs routed to it. Within seconds, the logic analyzer is ready to take a measurement. The MTC core, with its pin compression technology, reduces the number of required pins for tracing MicroBlaze processors by 50%.

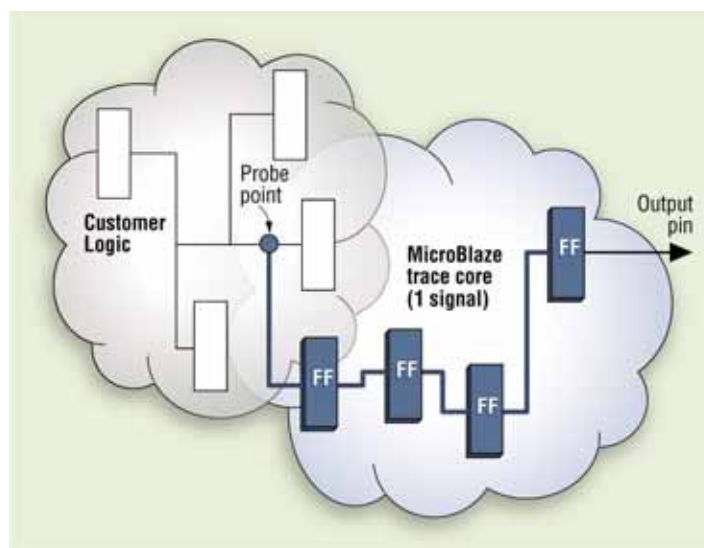


Figure 3 – The thick blue lines show the flops and routes added by the MTC core. Because there is a flop in the fabric – in addition to one at the I/O buffer – the router can use timing solely within the MTC core to move across the chip, thereby minimizing the impact of timing changes with the addition of the MTC core.

Conclusion

FPGAs enable fast, accurate processor execution tracing not available for stand-alone processors. Agilent's inverse assembler for the MicroBlaze soft-processor core provides you with an effective tool for tracing software execution. Agilent logic analyzers, equipped with precise time resolution, correlate MicroBlaze execution history with other software or hardware events acquired simultaneously. This allows you to quickly isolate problems associated with hardware and software interaction.

Agilent's royalty-free MTC core, distributed as part of the Xilinx Embedded Development Kit (beginning with version 8.1i), minimizes the time to set up measurement and eliminates the need for a specified PC board layout. For more information, visit www.agilent.com/find/microblaze.