A Paradigm Shift in Signal Integrity and Timing Analysis

Emerging high-speed interfaces are breaking traditional analysis approaches, forcing a paradigm shift in analysis tools and methodology.

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Simplistic rule-of-thumb approaches to interface analysis are proving to be woefully inadequate for analyzing modern high-speed interfaces like DDR2, PCI Express, and SATA-II. This situation will only worsen when emerging standards like DDR3 and 5-10 Gbps serial interfaces become commonplace.

Signal integrity analysis performed on only the shortest and longest nets in a design may not identify the worst-case inter-symbol interference, crosstalk, or pin timing scenarios caused by variations in stub length, number of vias, routing layers, AC specifications, package parasitics, and power delivery. An integrated, interface-centric approach that incorporates comprehensive signal integrity, timing, crosstalk, and power integrity analysis is required to more accurately predict system-level noise and timing margins.

Figure 1 offers the results of a simplistic versus comprehensive analysis approach to illustrate the shortcomings associated with some analysis tools, which are built on outdated rule-of-thumb methodologies and assumptions. The first waveform in Figure 1 represents a high-speed differential network using Xilinx® Virtex™-II ProX RocketIO™ IBIS models, lossless transmission lines, and ideal grounds with no crosstalk or power noise.

It is quite apparent from viewing the results that the simplistic analysis approach fails to provide the accuracy of the more comprehensive approach. The second waveform represents the progressive effect on the eye as a longer stimulus pattern is used, along with more accurate modeling of interconnect structures. The analysis also used detailed SPICE I/O models, accounting for power delivery, crosstalk, non-ideal grounds, and variations in process, voltage, and temperature.

When designers are fighting for tens of picoseconds and tens of millivolts, an approach that considers all of the factors affecting margin (see Figure 2) is essential to ensure that a design will meet its cost and performance goals.

Model Interconnect Topologies and Termination Schemes

Accurate modeling of interconnect structures and termination – including the component packaging, PCBs, connectors, and cabling – is critical for accurate simulations of high-speed networks. As edge rates have increased and interconnect structures have remained relatively long, the importance of modeling frequency-dependent loss has become much more crucial, which requires the use of two- and three-dimensional field solvers. Given the potential for wide varia-

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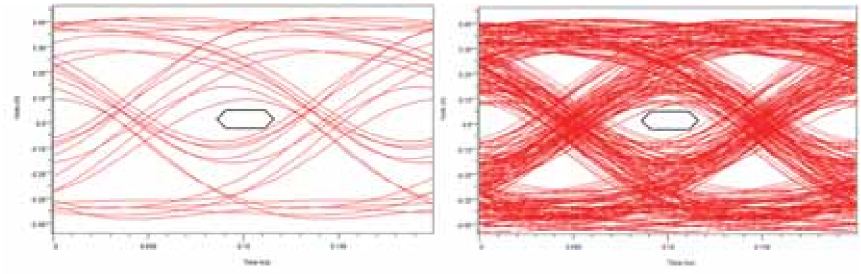

Figure 1 – Xilinx Virtex-II RocketIO transceiver simplistic versus comprehensive analysis

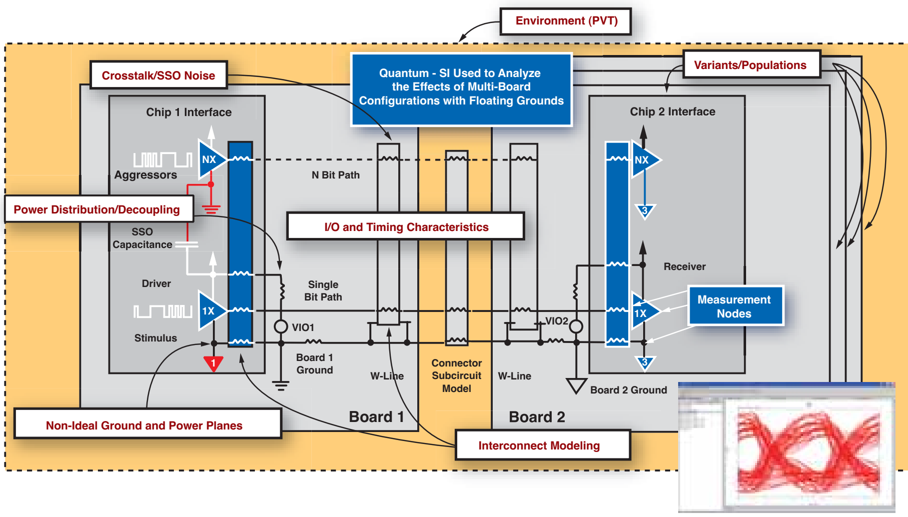

Figure 2 – Factors affecting system-level noise and timing margins

tion in the physical routing through packaging, PCBs, connectors, and cabling of many bus implementations, it is virtually impossible to identify the worst-case net without performing a comprehensive analysis on the entire interface.

Common analysis considerations that affect the analysis results include:

- Lossy versus lossless transmission lines
- Modeling vias as single- or multi-port structures
- Sensitivity to the number of vias in a net
- The use of two-dimensional distributed or three-dimensional lumped models for packages and connectors
- Modeling with S-parameters

Account for Inter-Symbol Interference

Traditional simulation approaches assume that signals are quiescent before another transition occurs. As the operating frequencies increase, the likelihood that a line has not settled to its quiescent state increases. The effect on one transition from the residual ringing on the line from one or more previous transitions results in delay variations. These delay variations, called inter-symbol interference, or ISI, require complex stimulus patterns that excite the different resonances of the network to create the worst-case scenarios. For some networks, these patterns may have a handful of transitions, but for multi-gigabit serial links, it is common to use long pseudo-random bit sequence (PRBS) patterns. Because the resonant frequency of a network is a function of the electrical length, the worst-case ISI effects may or may not occur on the shortest or longest net. In addition, interconnect process variations must be accurately accounted for, as this variation will cause changes in the resonant frequency (reflections) of the network.

Multi-gigabit serial link interfaces contain embedded clocks in the serial stream and use clock recovery techniques to extract the serial data, which must meet stringent eye mask requirements. I/O buffer model accuracy that reflects pre-emphasis/de-emphasis and equalization is crucial for analyzing the effects of ISI.

Don't Forget the Effects of Crosstalk

Crosstalk is noise generated on a net from transitions on nearby interconnects in the circuit board, packages, connectors, and cables. Crosstalk can change the level of the signal on a net and therefore cause variations in the interconnect delays and reduce noise margins. Synchronous and asynchronous crosstalk are noise sources that must be fully analyzed to determine their effects on signal integrity and timing margins.

Model I/O Buffer Characteristics and Component Timing

I/O buffer electrical and timing characteristics play a key role in defining the maximum frequency of operation. A flexible methodology and automated analysis approach is required to support the wide variations in I/O technology models, including mixed IBIS and SPICE simulation. SPICE models are more accurate and very useful when simulating silicon-to-silicon. SiSoft implements this through its Core-to-Core Methodology, as shown in Figure 3. However, you should recognize that the improvement in accuracy comes at a price – a 5x to 100x simulation speed decrease.

Output buffers and input receivers are commonly characterized by numerous electrical/timing characteristics and reliability thresholds. These cells may include on-die termination, controlled impedances/slew rates, pre-emphasis, and equalization.

For high-speed parallel buses, data input timing is defined as a setup/hold time requirement with respect to a clock or strobe. Data output timing is defined by the minimum and maximum delay when driving a reference load with respect to a clock or strobe. With the advent of SSTL signaling, AC and DC levels were introduced for Vil/Vih to more accurately characterize receiver timing with respect to an input signal. Further refinements have been made through slew rate derating (required for DDR2 and DDR3), which

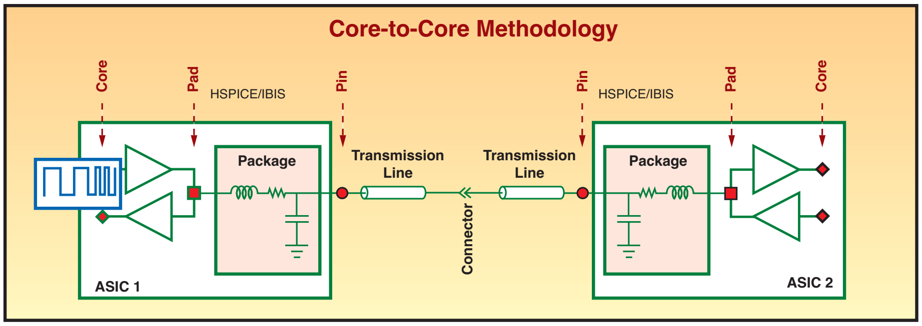

Figure 3 – SiSoft's Core-to-Core Methodology

uses tables to model the internal delay of a receiver at the core based on the slew rate at the pad. These refinements are not taken into account by simplified analysis approaches. This is why they cannot be used to accurately model the more complex behavior of many high-speed interfaces, where tens of picoseconds and tens of millivolts matter.

Don't Neglect PVT Variations

Many analysis tools and simplified methodologies neglect the effects of process, voltage, and temperature (PVT) variations, which can have disastrous results at high Mbps/Gbps signaling rates. It is especially important to consider IC process variations when modeling interconnect structures. Manufacturers typically supply data describing the AC specs and I/O buffer characteristics for fast, typical, and slow process parts, which bound the expected operating region. You should always analyze high-speed designs at the minimum/maximum operating extremes to avoid finding unpleasant surprises after the hardware is built.

Maintain Power Integrity

Maintaining the integrity of the power subsystems for both I/O and core power is critical. This requires analyzing stackups; PCB, package, and IC decoupling; routing layers and associated signal return paths. At a high level, the goal is to maintain a low impedance connection between associated voltage references across the operational frequency of interest. Simultaneous switching output (SSO) noise is commonly analyzed as part of power delivery to the I/O structures and also includes the effects of package crosstalk. SSO is often quantified in terms of a timing uncertainty penalty applied to the AC timing specs of the chip.

Accurately Determine Setup and Hold Margins

Faster interfaces require maintaining very tight timing margins. Interfaces are typically classified as either synchronous (common-clock), source-synchronous, clock recovery, or a hybrid of these types. It is important that the clock distribution is accurately simulated and used in carefully correlated ways with data nets to accurately predict timing margins and optimal clock distribution. The integration of accurate signal integrity, timing, crosstalk, and rules-driven design is the basis of a new paradigm, which we call "High-Speed Design Closure."

Required Tools and Methodology Paradigms

To overcome the shortcomings of traditional analysis methodologies and inaccuracies associated with oversimplified rules-of-thumb, today's high-speed interface designers need to adopt a more comprehensive interface-centric system-level analysis approach that addresses many (if not all) of the issues discussed in this article.

High-quality I/O buffer models, interconnect models, and accurate component AC timing/electrical specifications are fundamental to any analysis approach. The process of capturing and managing multiple interface designs; performing comprehensive simulations over process, voltage, and temperature for a large solution space of variables; and analyzing the simulation results for waveform quality, timing, crosstalk, SSO, and ISI effects is a daunting task without proper tools, which automate and integrate many manual steps and processes.

A highly automated analysis approach is also required to understand the loading effects associated with multi-board designs that include different board populations and part variants, and manage the complex set of variables within a multi-dimensional solution space. In pre-layout analysis, it is crucial to be able to mine the simulation results from different solution/space scenarios to pick an optimal solution for component placement and board routing.

Once the boards have been routed, it is equally important to verify the routed designs in the final system configuration, including different board populations and part variants to "close the loop" on signal integrity and timing. Accurate signal integrity analysis and crosstalk prediction in post-layout is essential to predicting system-level noise and timing margins.

With "High-Speed Design Closure," SiSoft is committed to providing tools for signal integrity, timing, crosstalk, and rules-driven design that meet rapidly changing signal integrity and timing requirements.

Conclusion

High-speed interface design and analysis complexity is only going to increase as edge rates and data rates get faster and voltage rails decrease. Engineering managers should recognize that setting up a high-speed interface analysis process requires an investment in simulation libraries, analysis products, and people.

When you invest in tools, do your homework first. Check to see if prospective tools can really address some of the tough issues presented in this article and that they provide you the growth path you need for the future. Perform thorough (and possibly lengthy) comparative evaluations of potential products to see if they address your current signal integrity, timing, power delivery, and crosstalk analysis needs, but also keep an eye to the future – it will arrive sooner than you think.

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