Deliver Efficient SPI-4.2 Solutions with Virtex-4 FPGAs

Virtex-4 devices offer an ideal platform for source-synchronous designs like the widely adopted SPI-4.2 interface.

by Chris Ebeling
Principal Engineer
Xilinx, Inc.
chris.ebeling@xilinx.com

Krista Marks
Sr. Manager, IP Solutions Division
Xilinx, Inc.
krista.marks@xilinx.com

SPI-4.2 (System Packet Interface Level 4 Phase 2) is the Optical Internetworking Forum's recommended interface for the interconnection of devices for aggregate bandwidths of OC-192 (ATM and POS) and 10 Gbps (Ethernet), as illustrated in Figure 1.

In the last few years, this interface has become the de-facto standard on all leading 10 Gbps framer ASSPs and has been implemented directly on many next-generation network processors. SPI-4.2 has been broadly adopted because of its efficient interface, which offers high bandwidth with a low pin count and seamless handling of typical system requirements such as flow control, error insertion/detection, synchronization, and bus re-alignment.

The Xilinx® Virtex-4™ architecture provides an ideal platform for implementing SPI-4.2. The Xilinx SPI-4.2 LogiCORE™ IP targeting Virtex-4 devices provides a solution with one-third less resources, dramatic power savings, 1+ Gbps LVDS double-data-rate (DDR) I/O, and complete pin assignment flexibility.

SPI-4.2 LogiCORE IP

Xilinx has improved on its Virtex-II™ and Virtex-II Pro™ SPI-4.2 solution, already one of the smallest in the industry, and made it 30% smaller by leveraging new ChipSync™ technology in the Virtex-4 FPGA. ChipSync technology is supported on every pin of the Virtex-4 device family; thus the new SPI-4.2 LogiCORE IP can be targeted to any device pin-out. This allows you to select I/O pins that best fit your system and PCB requirements.

In addition, for those applications requiring multiple SPI-4.2 interfaces, the Virtex-4 FPGA's logic density, high pin count, and extensive clocking resources will support four or more full-duplex cores in a single device. Regardless of the performance your application requires, Virtex-4 devices fully support the entire SPI-4.2 operating range, with high-speed LVDS support of data rates greater than 1 Gbps per pin.

ChipSync Technology

Xilinx introduced ChipSync technology in Virtex-4 FPGAs to enhance I/O capability when used for source-synchronous applications like SPI-4.2. ChipSync features are supported in every Virtex-4 I/O pin and include:

- New serial and de-serial (OSERDES and ISERDES) features. This enables logic built in the fabric to interface to the I/O at a fraction of the source-synchronous clock rate. The ISERDES also includes a Bitslip function. Bitslip allows you to shift the starting bit of deserialized data to achieve proper word alignment when linking multiple pins together (bus deskew).
- A new input delay (IDELAY) feature. This allows you to precisely adjust the input delay of each bit of a bus independently, in 78 ps increments. This provides a mechanism for tuning the interface timing to the system environment.

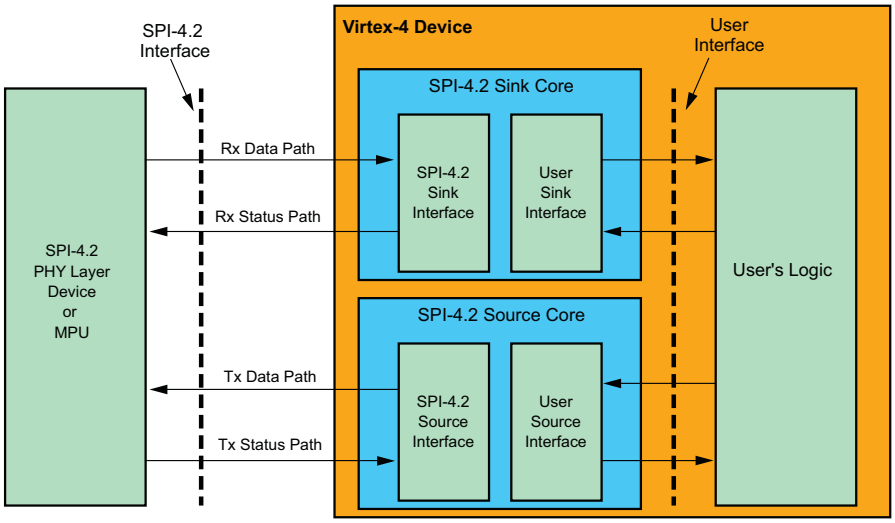

Figure 1 – Typical SPI-4.2 application

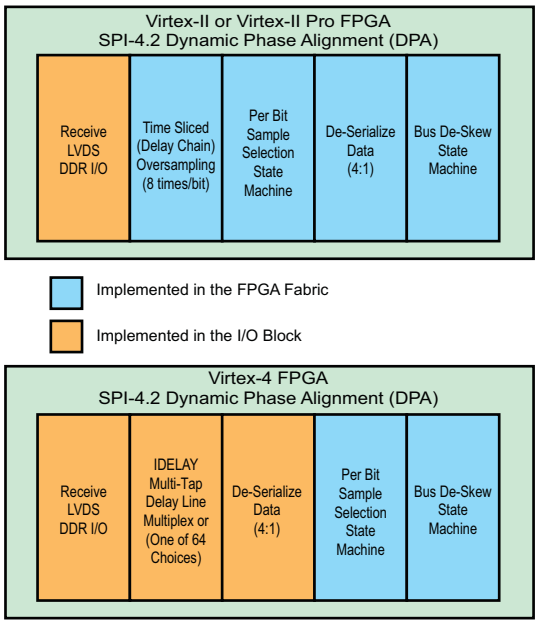

Figure 2 – DPA implementation in I/O logic for Virtex-II devices versus Virtex-4 devices

Additional DDR registers are now fully integrated into the input (ILOGIC) and output (OLOGIC) pins, simplifying the interface between the FPGA fabric and I/O blocks and supporting data transfer to and from the I/O logic on a single clock edge.

SPI-4.2 and ChipSync Technology

The SPI-4.2 interface has a DDR source-synchronous data bus that comprises 18 LVDS pairs (16 data bits, 1 control bit, and 1 clock). The SPI-4.2 source-synchronous clock varies from 311 MHz to 500 MHz.

For example, a typical OC-192 framer will require an aggregate bandwidth of 10 Gbps, which for a 16-bit dual data rate bus would require a data clock of at least 311 MHz, with 350 MHz a typical clock rate. The Xilinx SPI-4.2 LogiCORE IP easily meets your application requirements, regardless of performance, and with Virtex-4 ChipSync technology delivers a solution that is smaller and more flexible then prior FPGA implementations.

The SPI-4.2 core uses ChipSync technology to serialize egress data and de-serialize ingress data to a four-word (bus cycle) SPI-4.2 data stream at a lower clock rate. Operation of the core logic at a lower internal clock rate allows you to implement high-frequency SPI-4.2 interfaces in the slowest speed grade Virtex-4 device.

The ISERDES and OSERDES functions allow the core logic to time multiplex and de-multiplex these four words to and from the I/O logic without using any CLB logic resources. The core logic need only operate at half the source-synchronous DDR clock rate. For example, a SPI-4.2 interface with a 500 MHz DDR reference clock would only require an FPGA fabric clock of 250 MHz – easily achievable in the Virtex-4 architecture.

As the frequency of the source-synchronous clock increases, data recovery at the receiving (sink) device becomes more challenging. The SPI-4.2 protocol provides a calibration data, or training pattern, that permits a receiving device to adjust its data sampling to the system interface timing. The process of tuning the interface to its particular timing is referred to as dynamic phase alignment (DPA).

Before Virtex-4 devices, Xilinx DPA solutions worked by over-sampling the input data and choosing the best sample from the group. This required valuable FPGA resources and careful control of the input data path in the FPGA fabric, restricting the SPI-4.2 interface pin placement. In Virtex-4 FPGAs, the IDELAY feature present in every I/O is ideally suited to perform this function, as shown in Figure 2. (See "Dynamic Phase Alignment with ChipSync Technology in Virtex-4 FPGAs," also in this issue of the *Xcell Journal*).

The IDELAY features have two primary benefits for the SPI-4.2 core in Virtex-4 FPGAs:

- Integrating the IDELAY feature into the input pin (ILOGIC) reduces the FPGA resources required for DPA to less than 350 slices.
- The IDELAY function's ability to adjust the data sampling point enables DPA to be implemented in the I/O – except for a small control state machine, which is implemented in the fabric. The state machine portion is fully synchronous and does not require a complex macro. Thus, there are no restrictions on SPI-4.2 pin assignments.

Clocking Resources

Virtex-4 FPGAs provide an unprecedented number of clock resources for implementing multiple SPI-4.2 interfaces in a single device. With the Virtex-II and Virtex-II Pro architectures, implementing more than two SPI-4.2 interfaces posed a clock management challenge. The abundance and flexibility of clock distribution in the Virtex-4 family solves this challenge, supporting as many SPI-4.2 interfaces as the device logic and I/O will allow.

In Virtex-4 devices, all devices have 32 global clock resources. No restrictions exist on global clock distribution other than a maximum of eight global clocks per clock region. All clock regions have access to any 8 of the 32 total global buffers, regardless of the requirements of other clock regions.

In addition to the eight global clocks, each region in the device has two regional clock buffers. The regional clock resources are ideal for interface clocking, like the source-synchronous clock scheme used by SPI-4.2. Note that even the smallest Virtex-4 device has a total of 48 available clock resources, each designed for low-skew clock distribution and clock power management. The SPI-4.2 LogiCORE IP can be configured to use either global or regional clock resources.

In Virtex-4 FPGAs, the global clock trees and associated buffers are implemented differentially, for best duty-cycle fidelity and greater common-mode noise rejection. With Virtex-II and Virtex-II Pro devices, if SPI-4.2 interface operates above 350 MHz, you must route the high-speed reference clock using two clock buffers to minimize duty-cycle distortion at the DDR registers.

Figure 3 – Illustration of four SPI-4.2 LogiCORE IP implemented on a Virtex-4 XC4VLX60 device

interfaces in the larger devices (Figure 3). The Virtex-4 clocking capability opens up a whole new class of SPI-4.2 applications, and provides an ideal platform for applications such as multiplexing and de-multiplexing, bridges, and switches.

	VIRTEX-II	VIRTEX-II PRO	VIRTEX-4
Power: Static Alignment @ 700 Mbps per LVDS Pair	1.9W	1.75W	1.55W
Power: Dynamic Alignment Performance per LVDS Pair	2.6W @800 Mbps	2.8W @944 Mbps	2.0W @1 Gbps
Speed Grades Supporting 800 Mbps per LVDS Pair	-6	-6, -7	-10, -11, -12

Table 1 – SPI-4.2 power estimates for Virtex-II, Virtex-II Pro, and Virtex-4 FPGAs

Because each global clock tree in Virtex-4 FPGAs is implemented differentially, only one clock buffer is required.

Not only does the Virtex-4 architecture have considerably more clock resources, but because they are distributed differentially, the SPI-4.2 LogiCORE IP requires fewer of them. These high-performance clock resources support as many as four SPI-4.2 interfaces in a mid-range device (LX40/LX60) and more than four SPI-4.2

Higher Performance at Lower Power

Virtex-4 silicon is manufactured with a triple-oxide process that reduces static power consumption by 40%. This will have a positive impact for all designs, including the SPI-4.2 interface, where the power savings are dramatic, as readily illustrated and summarized in Table 1.

With Virtex-4 devices, SPI-4.2 uses significantly less power than its Virtex-II and Virtex-II Pro predecessors, both because of the enhanced 90 nm semiconductor process and because the LogiCORE IP uses 30% less fabric resources. At the same time, Virtex-4 FPGAs support 30% higher internal performance for SPI-4.2, with a maximum frequency of 250 MHz in the lowest speed grade (compared to 175 MHz in the lowest speed grade of Virtex-II and Virtex-II Pro devices). In addition, Virtex-4 FPGAs support 1+ Gbps LVDS for every I/O on the device.

This means that not only can you place multiple SPI-4.2 interfaces anywhere on the device, but for each implemented interface you get an aggregate bandwidth as high as 16+ Gbps. Designs that do not require this level of performance (such as more typical framer interfaces running at 10-12 Gbps) automatically get additional performance overhead that ensures ease of design integration and timing closure.

Conclusion

The Xilinx SPI-4.2 LogiCORE IP, coupled with Virtex-4 features, provides a highly efficient SPI-4.2 solution. We developed ChipSync technology that supports every I/O pin specifically for source-synchronous interfaces like SPI-4.2.

This technology enables you to design the most efficient SPI-4.2 solution, which uses significantly less resources (35% less), allows fully flexible device pin assignments (you choose the pinout), and supports extremely high interface speeds (1+ Gbps LVDS DDR I/O).

The higher performance is even more compelling because Virtex-4 FPGAs deliver it with lower power and significantly higher internal operating rates. The wealth of Virtex-4 clocking resources, combined with full pin assignment flexibility, opens up the possibility for new applications with multiple SPI-4.2 interfaces.

For more information about SPI-4.2 LogiCORE IP targeting Virtex-4 devices, please refer to this site at the Xilinx IP Center: *www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=DO-DI-POSL4MC*. A hardware demonstration is also available; for more information, contact your Xilinx representative.