

Introduction

The LogiCORE™ Virtex-4 Embedded Tri-mode Ethernet Media Access Controller (MAC) Wrapper automates the generation of HDL wrapper files for the Embedded Tri-Mode Ethernet MAC in Virtex-4™ FX devices using the CORE Generator™ tool.

VHDL and Verilog instantiation templates are available in the Libraries Guide for the Virtex-4 Ethernet MAC primitive; however, due to the complexity and the large number of ports, the CORE Generator simplifies integration of the Ethernet MAC by providing HDL examples based on user-selectable configurations.

Features

- Allows selection of one or both of the two Ethernet MACs (EMAC0/EMAC1) from the Embedded Ethernet MAC primitive
- Connects the EMAC0/EMAC1 Tie-off Pins based on user options
- Provides user-configurable Ethernet MAC physical interfaces
 - Supports MII, GMII, RGMII v1.3, RGMII v2.0, SGMII, and 1000BASE-X PCS/PMA interfaces
 - Instantiates clock buffers, DCMs, RocketIOs, and logic as required for the selected physical interfaces
- Provides a simple FIFO-loopback example design, which is connected to the MAC client interfaces
- Provides a simple demonstration test bench based on the selected configuration
- Includes an example of a low-level driver for DCR accesses
- Generates VHDL or Verilog

LogiCORE Facts	
Supported Family	Virtex™-4 FX ¹
Performance	10 Mbps, 100 Mbps, 1 Gbps
Example Design Resources	
Slices	422-1354 ²
LUTs	464-1706 ²
FFs	519-1530 ²
BRAMs	4-8 ²
DCM	0-2 ²
BUFG	2-8 ²
Wrapper Highlights	
Optimized Clocking Logic	HDL Example Design
Hardware Verified	Demonstration Test Bench
Provided with Wrapper	
Documentation	Product Specification Getting Started Guide User Guide ³
Design File Formats	HDL Example Design, Demonstration Test Bench, Scripts
Constraints File	User Constraints File (.ucf)
Example Designs	Example FIFO connected to client I/F Demonstration Test Environment
Design Tool Requirements	
Supported HDL	VHDL and/or Verilog
Synthesis	XST 8.1i
Xilinx Tools	ISE™ 8.1i
Simulation tools	Mentor ModelSim® 6.1b Cadence IUS ⁴

1. Virtex-4 FX solutions require the latest silicon stepping and are pending hardware validation.
2. The precise number depends on user configuration; see [Device Utilization](#).
3. The Virtex-4 Embedded Tri-Mode Ethernet MAC User Guide is available from www.xilinx.com/bvdocs/userguides/ug074.pdf.
4. Scripts provided for Mentor ModelSim and Cadence IUS only.

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