

## Introduction

The Xilinx LogiCORE™ XAUI core is a high-performance, low pin count 10 Gbps interface intended to allow physical separation between data-link layer and physical layer devices in a 10-Gigabit Ethernet system.

The XAUI core implements a single-speed full-duplex 10 Gbps Ethernet eXtended Attachment Unit Interface (XAUI) solution for the Xilinx Virtex™-II Pro and Virtex-4 families of FPGAs.

The Virtex™-II Pro and Virtex-4 FPGA families, in combination with the XAUI core, enable the design of XAUI-based interconnects whether chip-to-chip, over backplanes, or connected to 10-Gigabit optical modules.

## Features

- Designed to 10-Gigabit Ethernet specification IEEE 802.3ae-2002
- Uses 4 RocketIO™ transceivers at 3.125 Gbps line rate to achieve 10 Gbps data rate
- Implements DTE XGXS, PHY XGXS, and 10GBASE-X PCS in a single netlist
- Uses Virtex-II Pro or Virtex-4 Digital Clock Management to implement optional XGMII interface clocking
- Uses Virtex-II Pro or Virtex-4 DDR I/O primitives for the optional XGMII interface
- Elastic buffering of inbound XGMII data (optional)
- Uses RocketIO transceivers for the XAUI interface
- 802.3ae-2002 Clause 45 MDIO interface (optional)
- 802.3ae-2002 Clause 48 State Machines (optional for Virtex-II Pro)
- Supports 10-Gigabit Fibre Channel (10-GFC) XAUI data rates and traffic
- Available under the [SignOnce IP Site License](#) program

LogiCORE Facts				
Core Specifics				
Supported Device Family	Virtex-II Pro -6, -7 (2VP4 or larger) Virtex-4 <sup>1</sup> (4VFX60)			
Resources Used <sup>2</sup>	Slices	LUTs	FFs	Block RAMs
	917	1327	700	0
Special Features	Delivered through the CORE Generator™			
Provided with Core				
Documentation	Product Specification Getting Started Guide User Guide			
Design File Formats	NGC netlist			
Constraints File	UCF			
Verification	VHDL test bench Verilog test fixture			
Example design	VHDL and Verilog			
Additional Items	UniSim-based simulation models			
Design Tool Requirements				
Xilinx Implementation Tools	ISE™ 8.1i			
Simulation	Mentor ModelSim® Cadence IUS			
Support				
Provided by Xilinx, Inc. a <a href="http://www.xilinx.com/support/">www.xilinx.com/support/</a>				

1. Virtex-4 FX solutions require the latest silicon stepping and are pending hardware validation.
2. Figures quoted are approximate for Virtex-II Pro default configuration. See "Device Utilization" on page 13 for details on device utilization by configuration.

© 2006 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners. Xilinx is providing this design, code, or information "as is." By providing the design, code, or information as one possible implementation of this feature, application, or standard, Xilinx makes no representation that this implementation is free from any claims of infringement. You are responsible for obtaining any rights you may require for your implementation. Xilinx expressly disclaims any warranty whatsoever with respect to the adequacy of the implementation, including but not limited to any warranties or representations that this implementation is free from claims of infringement and any implied warranties of merchantability or fitness for a particular purpose.