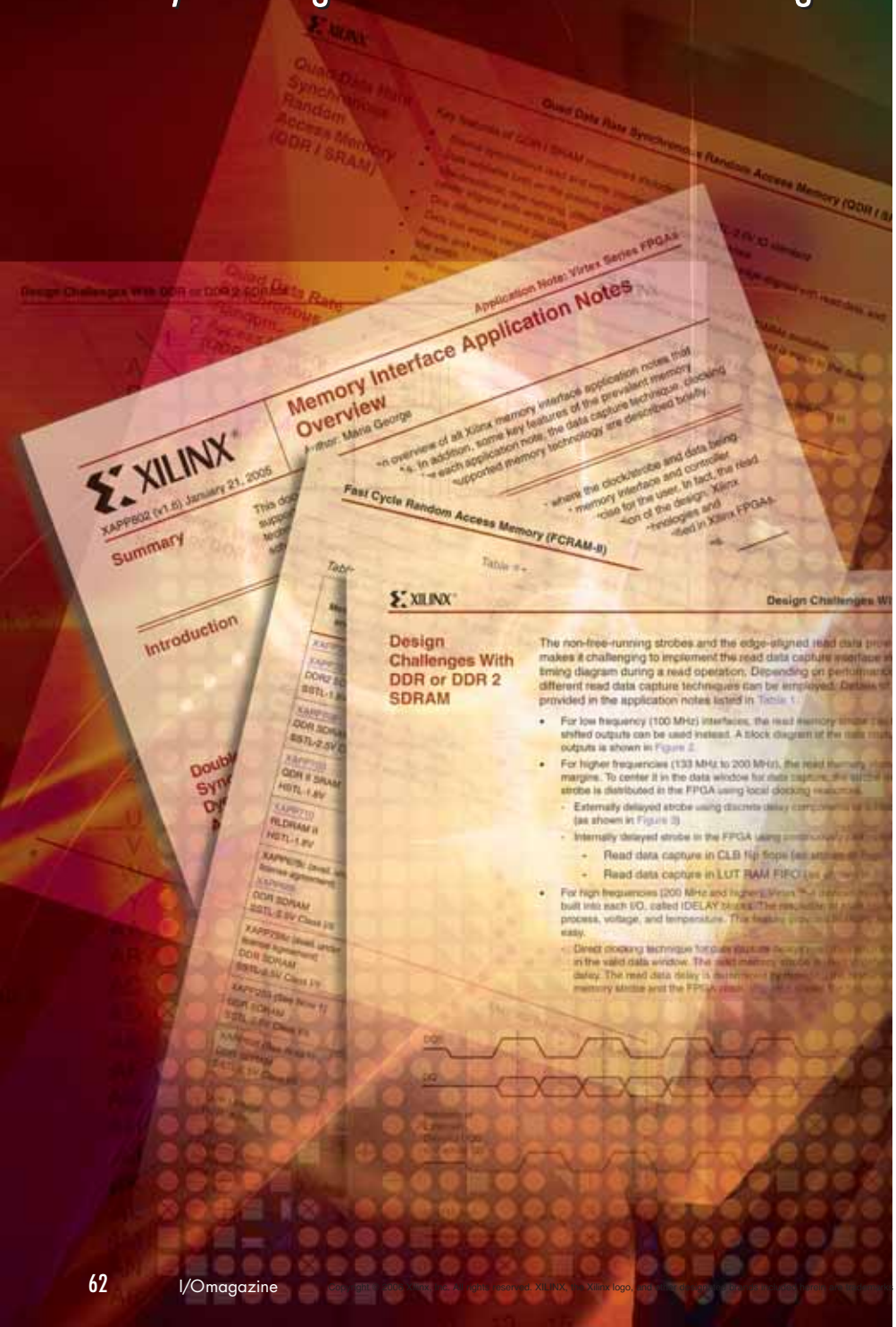
Memory Interfaces Reference Designs

Give your designs the Virtex-4 FPGA advantage.



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Memory interfaces are source-synchronous interfaces in which the clock/strobe and data being transmitted from a memory device are edge-aligned. Most memory interface and controller vendors leave the read data capture implementation as an exercise for the user. In fact, the read data capture implementation in FPGAs is the most challenging portion of the design. Xilinx provides multiple read data capture techniques for different memory technologies and performance requirements. All of these techniques are implemented and verified in Xilinx® FPGAs.

The following sections provide a brief overview of prevalent memory technologies.

Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM)

Key features of DDR SDRAM memories include:

- Source-synchronous read and write interfaces using the SSTL-2.5V Class I/II I/O standard
- Data available both on the positive and negative edges of the strobe
- Bi-directional, non-free-running, single-ended strobes that are output edge-aligned with read data and must be input center-aligned with write data
- One strobe per 4 or 8 data bits
- Data bus widths varying between 8, 16, and 32 for components and 32, 64, and 72 for DIMMs
- Supports reads and writes with burst lengths of two, four, or eight data words, where each data word is equal to the data bus width
- Read latency of 2, 2.5, or 3 clock cycles, with frequencies of 100 MHz, 133 MHz, 166 MHz, and 200 MHz
- Row activation required before accessing column addresses in an inactive row
- Refresh cycles required every 15.6 µs
- Initialization sequence required after power on and before normal operation

Double Data Rate Synchronous Dynamic Random Access Memory (DDR 2 SDRAM)

Key features of DDR 2 SDRAM memories, the second-generation DDR SDRAMs, include:

- Source-synchronous read and write interfaces using the SSTL-1.8V Class I/II I/O standard
- Data available both on the positive and negative edges of the strobe
- Bi-directional, non-free-running, differential strobes that are output edge-aligned with read data and must be input center-aligned with write data
- One differential strobe pair per 4 or 8 data bits
- Data bus widths varying between 4, 8, and 16 for components and 64 and 72 for DIMMs
- Supports reads and writes with burst lengths of four or eight data words, where each data word is equal to the data bus width
- Read latency is a minimum of three clock cycles, with frequencies ranging from 200 MHz to 400 MHz
- Row activation required before accessing column addresses in an inactive row
- Refresh cycles required every 7.8 µs
- Initialization sequence required after power on and before normal operation

Quad Data Rate Synchronous Random Access Memory (QDR II SRAM)

Key features of QDR II SRAM memories, the second-generation QDR I SRAMs, include:

- Source-synchronous read and write interfaces using the HSTL-1.8V I/O standard
- Data available both on the positive and negative edges of the strobe
- Uni-directional, free-running, differential data/echo clocks that are edge-aligned with read data and center-aligned with write data
- One differential strobe pair per 8, 9, 18, 36, or 72 data bits
- Data bus widths varying between 8, 9, 18, 36, and 72 for components (no QDR II SDRAM DIMMs available)

Memory Technology and I/O Standard	Supported FPGAs	Maximum Performance	Maximum Data Width	XAPP Number	XAPP Title	Data Capture Scheme
DDR 2 SDRAM SSTL-1.8V Class II	Virtex-4	333 MHz	8 bits (Components)	XAPP721 XAPP723	High Performance DDR 2 SDRAM Interface Data Capture Using ISERDES and OSERDES DDR2 Controller (267 MHz and Above) Using Virtex-4 Devices	Read data is captured in the delayed DQS domain and transferred to the FPGA clock domain within the ISERDES.
DDR 2 SDRAM SSTL-1.8V Class II	Virtex-4	267 MHz	16 bits (Components) 144-bit Registered DIMM	XAPP702 XAPP701	DDR 2 SDRAM Controller Using Virtex-4 Devices Memory Interfaces Data Capture Using Direct Clocking Technique	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay.
DDR SDRAM SSTL-2.5V Class I/II	Virtex-4	200 MHz	16 bits (Components) 144-bit Registered DIMM	XAPP709	DDR SDRAM Controller Using Virtex-4 Devices	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay.
QDR II SRAM HSTL-1.8V	Virtex-4	300 MHz	72 bits (Components)	XAPP703	QDR II SRAM Interface	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay.
RLDRAM II HSTL-1.8V	Virtex-4	300 MHz	36 bits (Components)	XAPP710	Synthesizable CIO DDR RLDRAM II Controller for Virtex-4 FPGAs	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay.

Table 1 – Virtex-4 memory interface application notes (XAPPs) currently available, with a brief description of the read data capture technique

XAPP Number Memory Technology and I/O Standard	Performance	Number of DCMs/DLLs	Number of BUFGs	Number of Interfaces with Listed DCMs and BUFGs	Device(s) Used for Hardware Verification	Requirements
XAPP721 XAPP723 DDR2 SDRAM SSTL-1.8V Class II	333 MHz	1 DCM 2 PMCDs	6	Multiple at Same Frequency	XC4VLX25 -11 FF668	All Banks Supported
XAPP702 XAPP701 DDR2 SDRAM SSTL-1.8V Class II	267 MHz	1	6	Multiple at Same Frequency	XC4VLX25 -11 FF668	All Banks Supported
XAPP709 DDR SDRAM SSTL-2.5V Class I/II	200 MHz	1	6	Multiple at Same Frequency	XC4VLX25 -11 FF668	All Banks Supported
XAPP703 QDR II SRAM HSTL-1.8V	300 MHz	1	3	Multiple at Same Frequency	XC4VLX25 -11 FF668	All Banks Supported
XAPP710 RLDRAM II HSTL-1.8V	300 MHz	1	5	Multiple at Same Frequency	XC4VLX25 -11 FF668	All Banks Supported

Table 2 – Resource utilization for all Virtex-4 memory interface application notes currently available

- Reads and writes with burst lengths of two or four data words, where each data word is equal to the data bus width
- Read latency is 1.5 clock cycles, with frequencies from 154 MHz to 300 MHz
- No row activation, refresh cycles, or initialization sequence after power on required, resulting in more efficient memory bandwidth utilization

Reduced Latency Dynamic Random Access Memory (RLDRAM II)

Key features of RLDRAM II memories include:

- Source-synchronous read and write interfaces using the HSTL-1.8V I/O standard
- Data available both on the positive and negative edges of the strobe
- Uni-directional, free-running, differential memory clocks that are edge-aligned with read data and center-aligned with write data
- One strobe per 9 or 18 data bits
- Data bus widths varying between 9, 18, and 36 for components and no DIMMs
- Supports reads and writes with burst lengths of two, four, or eight data words, where each data word is equal to the data bus width
- Read latency of five or six clock cycles, with frequencies of 200 MHz, 300 MHz, and 400 MHz
- Data-valid signal provided by memory device
- No row activation required; row and column can be addressed together
- Refresh cycles required every 3.9 µs
- Initialization sequence required after power on and before normal operation

Conclusion

For application notes on various memory technologies and performance requirements, visit *www.xilinx.com/memory*. The summaries in Table 1 and Table 2 can help you determine which application note is relevant for a particular design.