

Interfacing QDR II SRAM with Virtex-4 FPGAs

QDR II SRAM devices provide a suitable solution for memory requirements when partnered with Virtex-4 FPGAs.

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The growing demand for higher performance communications, networking, and DSP necessitates higher performance memory devices to support such applications. Memory manufacturers like Cypress have developed specialized memory products such as quad data rate II (QDR II) SRAM devices to optimize memory bandwidth for a specific system architecture. In this article, I'll provide a general outline of a QDR II SRAM interface implemented in a Xilinx® Virtex™-4 XC4VP25 FF6688-11 device.

Figure 1 shows a block diagram of the QDR II SRAM design interface, with the physical interface to the actual memory device on the controller.

QDR II SRAM

QDR II can perform two data write and two data reads per clock cycle. It uses one port for writing data and one port for reading data. These unidirectional ports support simultaneous reads and writes and allow back-to-back transactions without the bus contention that may occur with a single bidirectional data bus.

Clocking Scheme

The FPGA generates all of the clock and control signals for reads and writes to memory. The memory clocks are typically generated using a double-data-rate (DDR) register. A digital clock manager (DCM) generates the clock and its inverted version. This has two advantages. First, the data, control, and clock signals all go through similar delay elements while exiting the FPGA. Second, the clock-duty cycle distortion is minimal when global clock nets are used for the clock and the 180° phase-shifted clock.

The reference design uses the phase-shifted outputs of the DCM to clock the interface on the transmit side. This configuration gives the best jitter and skew characteristics.

QDR II devices include the following features:

- Maximum frequency of operations - 250 MHz - tested up to 278 MHz
- Available in QDR II architecture with burst of 2 or 4
- Supports simultaneous reads/writes and back-to-back transactions without bus contention issues
- Supports multiple QDR II SRAM devices on the same bus to:
 - Increase the density of the memory resource
 - Divide the speed of the interface by using multiple devices to achieve a given bandwidth

- Read: valid window worst-case 440 ps
- Write: valid window worst-case 460 ps
- Address and control signal timing analysis: command window worst-case 2360 ps

Conclusion

For more information about QDR II and Virtex-4 devices, see Xilinx application note XAPP703, "QDR II SRAM Interface for Virtex-4 Devices," at www.xilinx.com/bvdocs/appnotes/xapp703.pdf, as well as Cypress application note "Interfacing QDR-II SRAM with Virtex-4 Devices" at www.cypress.com.

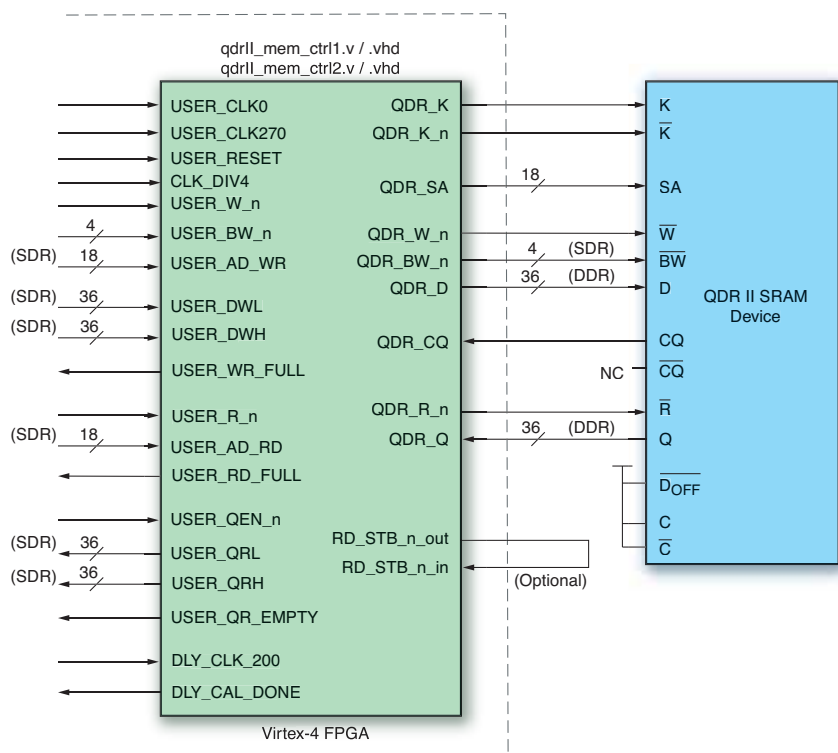


Figure 1 - Top-level architecture block diagram