



Xilinx PCI Express Solution

PCI Express has emerged as the next generation technology replacing PCI. It provides higher performance and increased bandwidth while maintaining the flexibility and familiarity of PCI. Despite the advantages of PCI Express, design challenges associated with this new and complex protocol will directly affect time-to-market.

Xilinx provides a range of FPGA solutions to meet the needs of a variety of PCI Express applications. The breakthrough Virtex-4 and Virtex-II Pro FPGAs offer a fully integrated solution for applications with limited board real estate, utilizing built-in transceivers to implement the entire PCI Express interface in a single device. Alternatively, the low-cost Spartan-3 and Spartan-3E FPGA families can be used along with an external PHY device via the PHY Interface for PCI Express (PIPE).



The Xilinx PCI Express Advantage

The Xilinx PCI Express solution includes the PCI Express 1-lane, 4-lane and 8-lane endpoint IP cores for use with the Virtex-4 and Virtex-II Pro FPGA devices and the PCI Express PIPE 1-lane endpoint IP core for use with the Spartan-3 and Spartan-3E FPGA devices.

High Performance – The RocketIO™ Multi-Gigabit Transceivers (MGTs) on the Virtex-4 and Virtex-II Pro FPGAs give this core a 2.5 Gbps line speed in 1-lane configuration, 10 Gbps line speed in 4-lane configuration and 20 Gbps live speed in 8-lane configuration.

Low-Cost – The Xilinx PCI Express PIPE endpoint core is a high-bandwidth scalable and reliable IP building block for use with the Spartan-3 and Spartan-3E FPGAs. It is ideally suited for a broad range of high volume computing and communications applications requiring a low cost and 100% compliance with the PCI Express Base Specification v1.1a.

Flexibility – The inherently programmable nature of the FPGA allows you to continually modify your design as your performance and interoperability requirements evolve, reducing your risk in adopting the new PCI standard.



General Features

- High-performance, highly flexible, scalable, reliable, and general purpose I/O core
 - Compliant to the PCI Express Base Specification v1.1a
 - Compatible with current PCI software model
- Fully compliant with PCI Express transaction ordering rules
- Supports removal of corrupted packets for error detection and recovery
- Design verified by Xilinx proprietary test bench

PCI Express 1-Lane, 4-Lane and 8-Lane Endpoint Cores

- Incorporates Xilinx Smart-IP™ technology to guarantee critical timing
- Uses the RocketIO Multi-Gigabit Transceivers on the Virtex-4 and Virtex-II Pro FPGA devices to achieve high transceiver capability
 - 2.5 Gbps per lane line speed
 - Supports 1-lane, 4-lane and 8-lane operation (8-lane on Virtex-4 only)
 - Elastic buffers and clock compensation
 - Automatic clock data recovery
- 8b/10b encode and decode
- Offers standardized user interface
 - Easy-to-use packet-based protocol
 - Full-duplex communication
 - Back-to-back transactions enable greater link bandwidth utilization
 - Supports flow control of data and discontinuation of an in-process transaction in the transmit direction
 - Supports flow control of data in the receive direction
 - Transaction traffic class selection enabled
 - Support for automatically handling of error forwarded packets
 - Automatically decodes and removes error forwarding packet indicator from received data
 - Forward compatible with future link widths

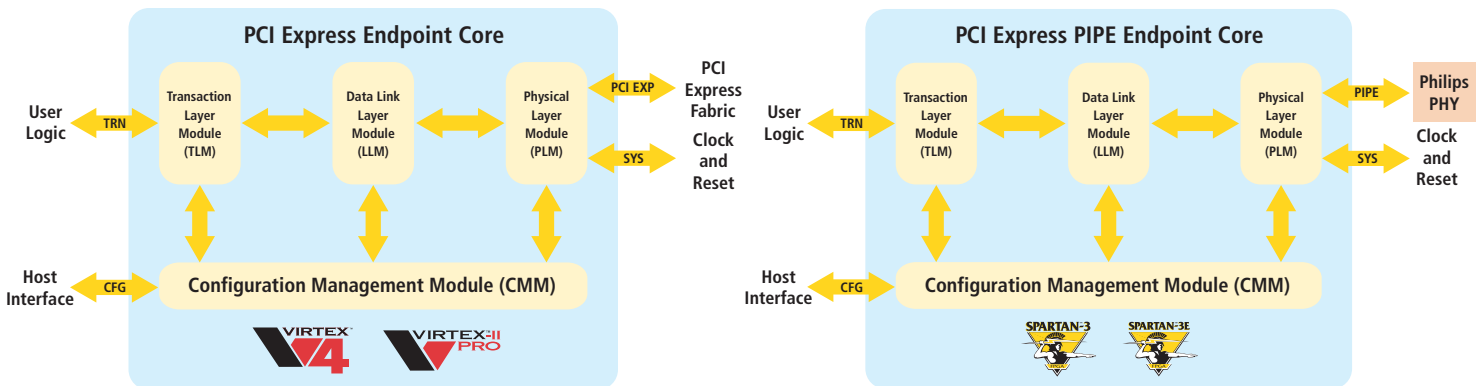
- Supports a maximum transaction payload of up to 4096 bytes
- Bandwidth scalability with frequency and/or interconnect width

PCI Express PIPE 1-Lane Endpoint Core

- Six individually programmable/configurable BARs and expansion ROM BAR
- Supports MSI and INTX emulation
- 32-Bit internal datapath
- Compatible with PCI/PCI-Express power management functions
 - Active state power management (ASPM)
 - Programmed power management (PPM)
- Used in conjunction with Philips PX1011A PCI Express standalone PHY to achieve high transceiver capability
 - 2.5 Gbps line speed
 - Elastic buffers and clock compensation
 - Automatic clock and data recovery
 - 8b/10b encode and decode
- Offers Xilinx-standardized easy-to-use LocalLink interface
 - Packet-based full-duplex communication
 - Back-to-back transactions enable greater link bandwidth utilization
 - Enables flow control of data and discontinuation of an in-process transaction in the transmit direction
 - Enables flow control of data in the receive direction
 - Automatically decodes and removes error forwarding packet indicator from received data
- Supports a maximum transaction payload of up to 512 bytes

Get Your PCI Express Solution Today

To learn more about the Xilinx PCI Express solution or to download the core, visit www.xilinx.com/pciexpress.



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