

Course Description

By learning PCI Express core protocol fundamentals, designers will gain a working knowledge of how PCI Express can be used in their systems. This course focuses on PCI Express protocol subjects that designers using the Xilinx PCI Express should understand in order to complete their designs faster and easier. Customers will also be introduced to each Xilinx PCI Express core product and will gain intimate knowledge of how the PCI Express core operates.

Level – Intermediate

Course Duration – 2 days

Price – \$1000 USD or 10 Training Credits

Course Part Number – PClxxxx-BETA

Who Should Attend? – Engineers who seek training in developing the necessary skills for designing PCI Express systems using Xilinx PCI Express cores

Prerequisites

- Basic PCI and/or PCI-X protocol knowledge
- Basic knowledge of Verilog or VHDL
- Basic experience with commonly used simulation tools like ModelSim
- Basic knowledge of Xilinx ISE™ software

Software Tools

- Xilinx ISE 8.1i
- ModelSim 6.0c PE

After completing this comprehensive training, you will have the necessary skills to:

- Effectively use the Xilinx PCI Express cores in your own design environments
- Select the appropriate PCI solution for a specific application
- Understand how PCI Express specification requirements apply to using Xilinx PCI Express cores.

Course Outline

Day 1

- PCI Express Overview
- Layers and Channels
- TLP Packet Fields and Packet Routing
- Local Link Interface
- **Lab 1:** Using the PCI Express Core Local Link Interface
- PCI Express Configuration Space
- **Lab 2:** Exploring the PCI Express Core Configuration Space

Day 2

- TLP Request and Completion Packets
- **Lab 3:** Designing with the PCI Express Core
- Physical Layer Electrical Subblock
- Physical Layer Logical Subblock
- Xilinx PCI Express Solutions
- **Lab 4:** Generating and Implementing a Xilinx PCI Express Core

Lab Descriptions

- **Lab 1:** Using the PCI Express Core Local Link Interface – This lab introduces the PCI Express core design that will also be used in Labs 2 and 3. It allows the user to become familiar with the cores user application interface (Local Link) and to modify the design to change the packets being sent
- **Lab 2:** Exploring the PCI Express Core Configuration Space – This lab reinforces lessons learned in the Configuration Space section by having users decode configuration packets to understand the requirements in configuring the core. In addition, users will be able to implement the user configuration space by modifying the Programmable I/O design receiver and transmit state machines
- **Lab 3:** Designing with the PCI Express Core – This lab takes an in-depth look at designing with the core. The user will become familiar with packet ordering, credits available, and allocating completion space for inbound completions
- **Lab 4:** Generating and Implementing a Xilinx PCI Express Core – This lab illustrates using the CORE Generator™ to generate a core. The core is then implemented and users can verify the implementation by studying the various reports created by Xilinx tools

Register Today

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and training credits.