Xilinx Configuration Memory Cross-Reference

Platform Flash/XL Flash Memory	
Virtex®-6 FPGAs	
XC6VLX75T	XCF32P
XC6VLX130T	XCF128X
XC6VLX195T	XCF128X
XC6VLX240T	XCF128X
XC6VLX365T	XCF128X
XC6VLX760	(2)XCF128X + CPLD
XC6VLX550T	(2)XCF128X + CPLD
XC6VSX315T	XCF128X
XC6VSX475T	(2)XCF128X + CPLD
XC6VHX250T	XCF128X
XC6VHX255T	XCF128X
XC6VHX380T	XCF128X
XC6VHX565T	(2)XCF128X + CPLD
Virtex-5 FPGAs	
XC5VLX30	XCF08P
XC5VLX50	XCF16P
XC5VLX85	XCF32P
XC5VLX110	XCF32P
XC5VLX155	XCF128X
XC5VLX220	XCF128X
XC5VLX330	XCF128X
XC5VLX20T	XCF08P
XC5VLX30T	XCF16P
XC5VLX50T	XCF16P
XC5VLX85T	XCF32P
XC5VLX110T	XCF32P
XC5VLX155T	XCF128X
XC5VLX220T	XCF128X
XC5VLX330T	XCF128X
XC5VSX35T	XCF16P
XC5VSX50T	XCF32P
XC5VSX95T	XCF128X or XCF32P[1]
XC5VSX240T	XCF128X
XC5VFX30T	XCF16P
XC5VFX70T	XCF32P
XC5VFX100T	XCF128X
XC5VFX130T	XCF128X
XC5VFX200T	XCF128X
XC5VTX150T	XCF128X
XC5VTX240T	XCF128X

Platform Flash/XL Flash Memory	
Spartan®-6 FPGAs	
XC6SLX4	XCF04S
XC6SLX9	XCF04S
XC6SLX16	XCF04S
XC6SLX25	XCF08P
XC6SLX25T	XCF08P
XC6SLX45	XCF16P
XC6SLX45T	XCF16P
XC6SLX75	XCF32P
XC6SLX75T	XCF32P
XC6SLX100	XCF32P
XC6SLX100T	XCF32P
XC6SLX150	XCF32P[1]
XC6SLX150T	XCF32P[1]
Virtex-4 FPGAs	
XC4VLX15	XCF08P
XC4VLX25	XCF08P
XC4VLX40	XCF16P
XC4VLX60	XCF32P
XC4VLX80	XCF32P
XC4VLX100	XCF32P
XC4VLX160	XCF32P + XCF08P
XC4VLX200	XCF32P + XCF32P
XC4VFX12	XCF08P
XC4VFX20	XCF08P
XC4VFX40	XCF16P
XC4VFX60	XCF32P
XC4VFX100	XCF32P
XC4VFX140	XCF32P + XCF16P
XC4VSX25	XCF16P
XC4VSX35	XCF16P
XC4VSX55	XCF32P

Platform Flash/XL Flash Memory	
Spartan-3A FPGAs	
XC3S50A	XCF01S
XC3S200A	XCF02S
XC3S400A	XCF02S
XC3S700A	XCF04S
XC3S1400A	XCF08P
Spartan-3A DSP FPGAs	
XC3SD1800A	XCF08P
XC3SD3400A	XCF16P
Spartan-3E FPGAs	
XC3S100E	XCF01S
XC3S250E	XCF02S
XC3S500E	XCF04S
XC3S1200E	XCF04S
XC3S1600E	XCF08P
Spartan-3 FPGAs	
XC3S50	XCF01S
XC3S200	XCF01S
XC3S400	XCF02S
XC3S1000	XCF04S
XC3S1500	XCF08P
XC3S2000	XCF08P
XC3S4000	XCF16P
XC3S5000	XCF16P

Notes: 1. Assumes typical compression benchmarks; compression should be confirmed using ISE® tools

Platform Flash Family Packages and Features							
Part Number	XCF01S	XCF02S	XCF04S	XCF08P	XCF16P	XCF32P	XCF128X
Density	1 Mb	2 Mb	4 Mb	8 Mb	16 Mb	32 Mb	128 Mb
JTAG Programmable	Yes	Yes	Yes	Yes	Yes	Yes	Indirect
Serial Configuration	Yes	Yes	Yes	Yes	Yes	Yes	No
SelectMAP Configuration	—	—	—	Yes	Yes	Yes	Yes
Compression	—	—	—	Yes	Yes	Yes	No
Design Rev	—	—	—	Yes	Yes	Yes	Yes
V_{CC} (V)	3.3	3.3	3.3	1.8	1.8	1.8	1.8
V_{CCO} (V)	1.8-3.3	1.8-3.3	1.8-3.3	1.8-3.3	1.8-3.3	1.8-3.3	2.5-3.3
V_{CCJ} (V)	2.5-3.3	2.5-3.3	2.5-3.3	2.5-3.3	2.5-3.3	2.5-3.3	N/A
Clock (MHz)	33	33	33	40	40	40	50
Standard Package	VO20	VO20	VO20	FS48	FS48	FS48	FT64
Pb-Free Package	VOG20	VOG20	VOG20	FSG48	FSG48	FSG48	FTG64
	—	—	—	VOG48	VOG48	VOG48	—

Notes: 1. The iMPACT software tool supports XCF128X JTAG programming indirectly via the Virtex-5 or Virtex-6 FPGA JTAG port.
2. For more information regarding design-in considerations of Platform Flash PROMs, refer to UG161, *Platform Flash User Guide* .

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Configuration Hardware Products

Platform Cable USB II - State-of-the-art Xilinx cable with industry-leading performance recommended for new designs. For in-system programming using Xilinx® iMPACT programming software connected via a simple four-wire header to the FPGA, PROM, or CPLD device on target board.

	Xilinx Download Cable Chart
Part Number	Platform Cable USB II
	HW-USB-II-G
Connection to PC	USB 1.1 (Basic Speed) or USB 2.0 (High-Speed)
I/O Voltage Support	1.5V, 1.8V, 2.5V, 3.3V, and 5V
Multiple Cable Management	Yes (Users can easily name and control individual cables through Xilinx iMPACT software)
Input Power Requirements	Bus Powered (+5VDC)
Configuration Modes	JTAG (IEEE Std 1149.1), Slave Serial, IEEE Std 1532, Direct SPI with automatic PROG_B control, Indirect programming of SPI and parallel flash memory devices (1)
Stand-Alone Programming Support	Download cable only
OS Support	Windows XP Professional (32 and 64 bit) Windows Vista (32 and 64 bit)
Xilinx Device Support	All Xilinx FPGAs, CPLDs, Platform Flash PROMs, XC18V00 PROMs, and System ACE™ Tool
Third-Party Flash Memory Support	Direct programming of specific SPI Flash memory devices (1) Indirect programming of specific SPI and parallel flash memory devices (1)
Device and Board Interface	Ribbon cable or flying wires (shipped with both)
RoHS Compliant	Yes
Miscellaneous	Improved target interface protection FPGA-based for feature growth Target system MUX control (PGND) for dynamic JTAG bus sharing
Maximum Target Clock Speed	12 MHz

Notes: 1. See XAPP951 for a list of SPI devices that Xilinx supports via direct programming and XAPP974 for a list of SPI devices that Xilinx supports via indirect programming

Key Configuration Solutions Application Notes

Design Guides for Configuration
Platform Flash XL User Guide - UG438
Platform Flash PROM User Guide - UG161
Bulletproof Configuration Best Practices Guide for Spartan®-3A FPGAs - XAPP986

Configuration Application Notes for In-System Programming and Remote Update
Xilinx In-System Programtming Using an Embedded Microcontroller, a microprocessor solution -XAPP058
Embedded In-System Programming, JTAG ACE Player Solution - XAPP424
Multiple-Boot with Platform Flash PROMs and Spartan-3E FPGAs - XAPP483
A CPLD-Based Configuration and Revision Manager for Xilinx Platform Flash PROMs and FPGAs - XAPP693
Updating a Platform Flash PROM Design Revision In-System Using SVF - XAPP972
Low-Profile In-System Programming Using XCF32P Platform Flash PROMs - XAPP975
MultiBoot with Virtex-5 FPGAs and Platform Flash XL - XAPP1100

Configuration Application Notes for Data Storage
Data storage with Platform Flash XCF02S/XCF04S PROMs - XAPP544

Configuration Application Note for Code Storage
MicroBlaze™ Processor Platform Flash/PROM Boot Loader and User Data Storage - XAPP482

Configuration Application Note for PCI/PCI-X
Dynamic Bus Mode Reconfiguration of PCI-X and PCI Designs - XAPP938

Configuration Application Notes for 3rd Party Flash Memory
A best-practices example using BPI flash for Virtex®-5 FPGAs configuration - XAPP973
A best-practices example using SPI flash for Spartan-3A FPGAs configuration - XAPP974

**To download these application notes, visit the 'Documentation' section at www.xilinx.com/products/design_resources/config_sol/

System ACE Technology

For multiple FPGA configuration and for designs utilizing system-level features, use the System ACE solution.

	System ACE Tool CF
Memory Density	Up to 8 Gb
Number of Components	2
Minimum Board Specifications	25 cm
Compression	No
FPGA Configuration Mode	JTAG
Multiple Designs	Unlimited
Software Storage	Yes
Removable	Yes
IRL Hooks	Yes
Maximum Configuration Speed	30 Mb/s
Nonvolatile Media	CompactFlash

Pb-free solutions are available. For more information about Pb-free solutions, visit www.xilinx.com/pbfree.

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Important: Verify all data in this document with the device data sheets found at www.xilinx.com