REDUCING BOM COSTS, JITTER, AND POWER REQUIREMENTS IN LARGE-CHANNEL-COUNT BROADCAST VIDEO EQUIPMENT

XILINX FPGA SERDES DYNAMIC PHASE INTERPOLATION FOR SDI DESIGNS: CLEAN REFERENCE CLOCKS WITHOUT THE EXPENSE OF EXTERNAL VCXOS

⟩ Broadcast Market Challenges

- Competitive pressures to lower switcher and router costs

- Demands for more bandwidth, resulting in equipment with large channel counts that drive up BOM costs and power requirements

- Need to meet stringent SDI jitter requirements and align/lock Tx to Rx reference clocks with high accuracy

- Need to do more with less, and protect investments in current designs

⟩ Xilinx Solutions

- Leverage in-design FPGAs to control SDI reference clocks without increasing power requirements

- Eliminate external VCXOs and simplify board layout for dramatically lower BOM costs and lower power

- Gain independently controlled output rates from all Tx transceivers

- Ability to lock to HSYNC signal for genlock needs without external PLLs

- Achieve lowest jitter, and decouple fabric noise from transceivers to achieve high signal integrity

Using traditional design methods, a production switcher or broadcast router can require dozens of voltage-controlled crystal oscillators (VCXOs) to allow FPGAs to pass through (SD/HD/3G-SDI) video channels. Priced at US$10-$15 each, the VCXOs add a significant and growing cost to the bill of materials (BOM) because video networking equipment is scaled up to carry large numbers of channels. The associated board complexity further increases costs, and the VCXOs can also draw 300-500mW per channel, adding costs to thermal management in the system. Xilinx now offers the ability to remove these external VCXOs from SDI designs. Each Virtex-6 and 7 series FPGAs transmit SERDES has a Transmit Clock Phase Interpolator (TXPI) for the transmit SERDES bit clock. Each Phase Interpolator in each transmit SERDES can be independently, dynamically, and continuously changed in phase and hence shifted in frequency to act as a replacement VCXO.

The Xilinx VCXO removal approach offers numerous benefits, including high signal integrity, and the freedom to use all transmit SERDES at completely independent rates. Taking advantage of an in-design Xilinx FPGA for this function also allows designers to minimize the power requirements for the complete system. The design is proven to work in hardware, and the Xilinx Virtex-6 FPGA Broadcast Connectivity Kit and 7 series platforms can be used to evaluate the VCXO removal reference design.

VCXO REPLACEMENT REFERENCE DESIGN
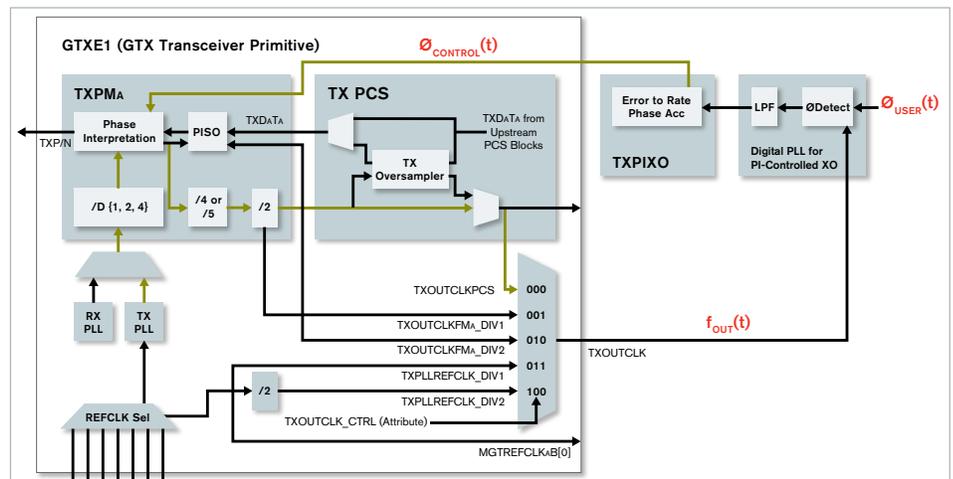
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Benefits of Xilinx TX SerDes Phase Interpolation for VCXO Replacement

- Dramatically reduces system BOM costs, particularly for large channel count designs
- 100% SERDES utilization (each SERDES has a Tx phase interpolator – no need to share frequencies across transceivers)
- Low jitter and compliance with SMPTE SDI specifications
- Decouples fabric noise from SERDES
- Jitter filter shape can be controlled in fabric
- Complete digital and dynamically phase shifting of line rate clock within the Tx SERDES)

- Avoids the need for extra power (300-500mW per external VCXO)
- Can lock to HSYNC for genlocking
- Works in slowest speed grade devices
- Avoids increasing global clock buffer (BUFG) resources
- Scales to 10Gbps designs
- Passes industry interoperability tests

VCXO-BASED DESIGNS COMPARED TO XILINX PHASE INTERPOLATION
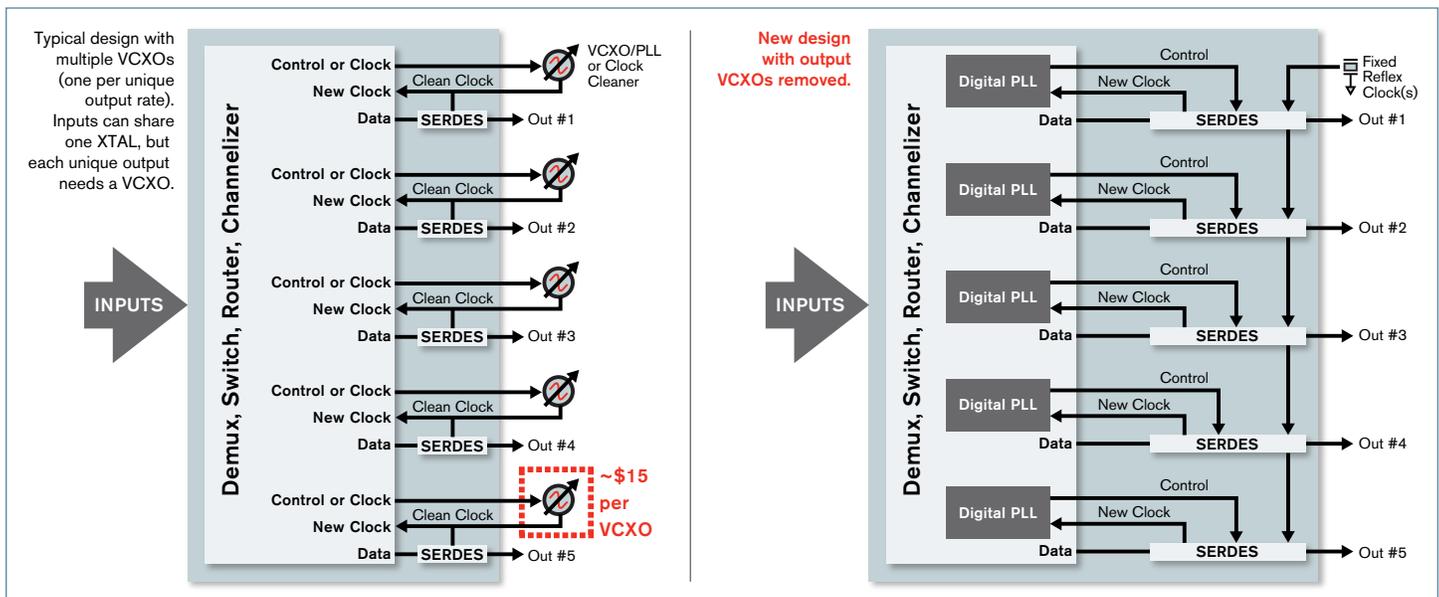
Take the NEXT STEP

To request a demo, please contact your local Xilinx sales representative, or email **broadcast@xilinx.com**

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