XILINX®

2011
INNOVATION

IP QUALITY

FPGA customers are faced with the increasing complexity of systems, time-to-market pressures, and the need to improve their engineering teams' productivity. The broad, feature-rich, high-quality Xilinx IP portfolio helps designers address these challenges. With the goal of driving up the quality of its silicon and IP, Xilinx initiated the company-wide Xilinx Verification Initiative (XVI) in 2009. XVI introduced a robust, common set of guidelines and best practices aligned with industry-leading development and verification standards. These XVI recommendations became a required Xilinx policy that has been adopted across all teams to ensure consistent, quality-focused IP testing processes and methodologies.

This report explains the resulting steps that Xilinx is now taking for improved quality of IP, and describes the benefits for the end users.

PROJECT DIRECTIVES

A yearly reduction of 10% in customer-triggered defect reports, and an improved out-of-box experience for Xilinx IP

Steps Taken

Combined efforts from a broad, cross-functional team have addressed several aspects of Xilinx IP development: IP generation, simulation, and implementation across multiple platforms, and third-party tools.

These efforts have yielded several enhancements:

- *Static checks such as RTL linting against coding policies and clock domain crossing checks*
- *A broad set of coverage metrics to track the verification and testing of IP, including functional coverage, code coverage, parameter coverage, and bug find/fix rates*
- *A new unified test flow to automate and standardize testing of different types of IP (e.g., Embedded Development Kit, CORE Generator™)*
- *Testing of IP on various Windows and Linux platforms, and with different simulators such as ISIM and third-party simulators*
- *"Automated IP Checker" dashboard to carry out checks pertaining to IP metadata*
- *A company-wide dashboard to report and track IP test status and convergence*
- *In addition to simulation verification, IP is hardware tested across a variety of Xilinx hardware validation platforms that span multiple families of devices.*
- *IP is tested and evaluated for ease of integration.*

CONT'D. >>

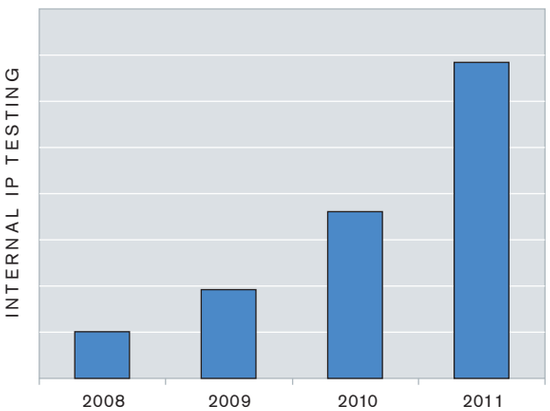
Results

The IP quality improvement efforts started with the goal of reducing customer-triggered defect reports by 10%. After two years and an extensive overhaul of IP development and testing infrastructure, Xilinx has achieved a reduction of more than 33% in customer-triggered defect reports relating to Xilinx IP.

Benefits

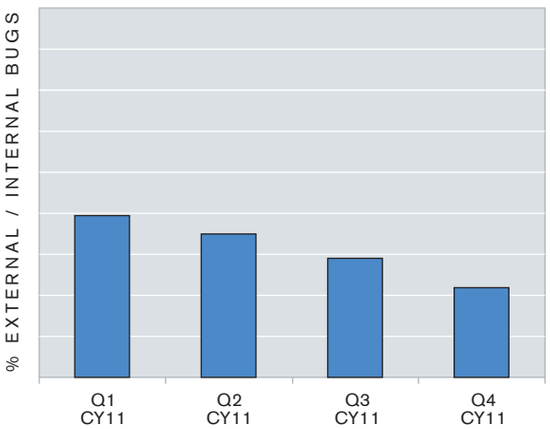
The improvement in Xilinx IP quality has helped customers in a number of ways. For example, using prevalidated customizable IP helps reduce the cost of development and shorten customers' time to market. As design complexity increases, the availability of ready-to-use, off-the-shelf IP helps Xilinx customers focus on integration and product differentiation rather than IP development.

Increased Testing Prevents Customer Issue Discovery



Xilinx IP verification methodology tracks industry design trends. Standardization and increased testing maximize issue identification and resolution prior to application by a customer.

Driving Fewer Customer-Discovered Bugs



Even with the increase in the breadth of the IP offering and the increased complexity of the IP, customers are discovering far fewer bugs. The vast majority of issues have been discovered and resolved earlier by Xilinx teams.

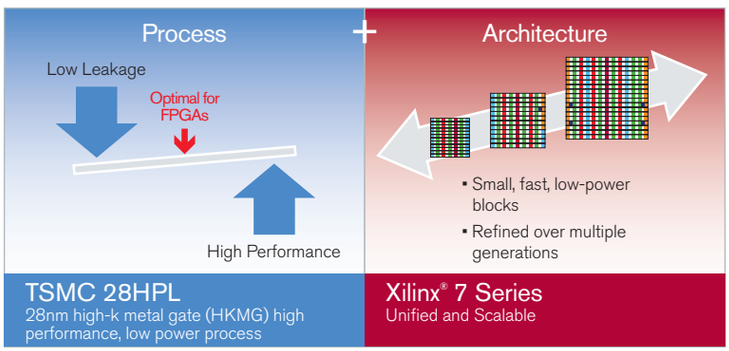
2011
INNOVATION

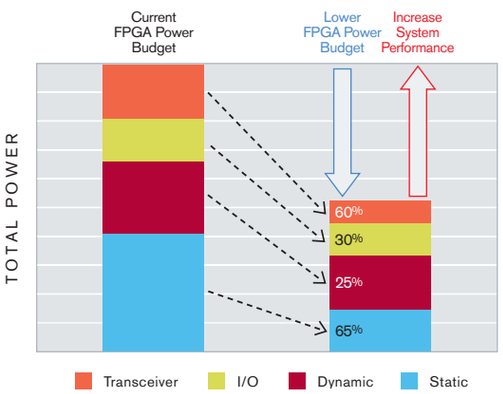
28nm:

Successful Launch and Continuous Innovations

The Xilinx focus on quality resulted in bringing the industry's first 28nm devices to market. The new product evaluation/new product introduction (NPE/NPI) steps started with the selection of the high-κ metal gate (HKMG) high-performance, low-power (HPL) fabrication process pioneered by Taiwan Semiconductor Manufacturing Co. (TSMC). During the five years of development, this node has proven to deliver a significant reduction in static power consumption, increased performance, and the highest quality. Using tools such as the Xilinx proprietary Process and Performance Learning Vehicle (PPLV), the technology has delivered on its promises.

In collaboration with the best-in-class wafer fabrication team at TSMC, Xilinx has complimented the 28nm process with the strength of a scalable optimized architecture. This architecture scales from the low-end Xilinx Artix™-7 products to the high-performance Virtex®-7 products and provides tremendous benefits in design portability and IP migration. Additionally, this new architecture has allowed Xilinx to streamline its introduction process for more predictable, high-quality results, earlier identification of errata, and more time to fix problems before production.



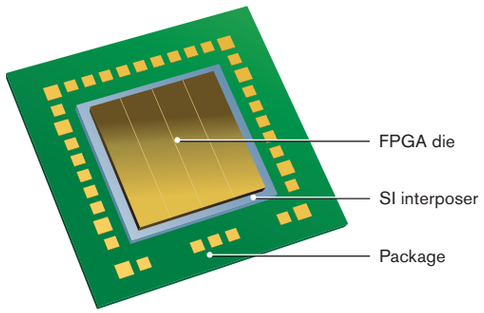


7 Series Innovations:
- Rearchitected Transceivers
- Multimode I/O Control
- Intelligent Clock Gating
- Power Binning and Voltage Scaling
- HPL Process

CONT'D. >>

Besides delivering the first 28nm devices, Xilinx has launched additional product platforms including the Zynq™-7000, the first ARM®-based FPGA, and the Virtex-7 2000T based on innovations in stacked-silicon interconnect technology. A passive interposer provides the interconnect between the multiple dice, which are referred to as Super Logic Regions (SLRs).

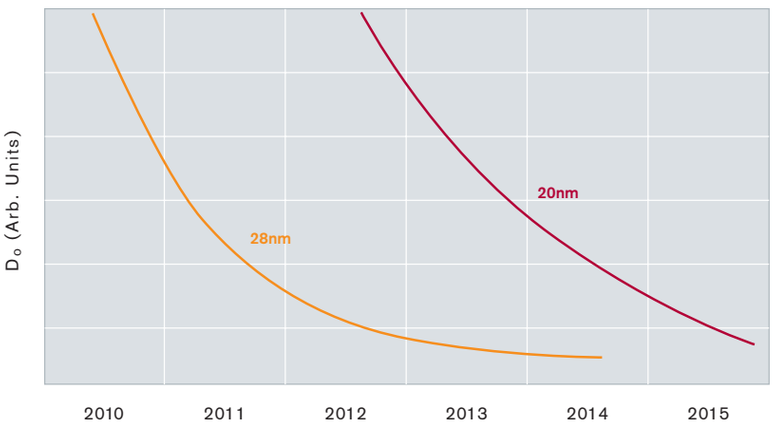
Xilinx's stacked-silicon interconnect (SSI) technology enables an FPGA with more resources (logic, memory, serial transceivers, and processing elements) as well as breakthrough capacity and performance bandwidth. SSI technology also makes it possible to combine multiple FPGA dice, resulting in a 100x improvement in interdie bandwidth per watt compared with conventional approaches.



20nm: Innovating the Next Node

Having accelerated and improved the development of the 28nm process, Xilinx is now using test chips for 20nm development. While still in early development, the test chips have already successfully overcome many process challenges. The PPLV offers many benefits, including added cycles of learning that improve quality earlier in the life cycle. Test chips and the scalable optimized architecture significantly speed time to market for FPGA devices, since they provide detailed process technology look-ahead in the areas of yield enhancement (better understanding of defects), performance predictability, and reliability.

Defect Density Levels for 28nm and 20nm Technology



Xilinx-pioneered innovations benefit from technologies previously proven in high-volume production, which lowers risks and can provide significant value to customers, partners, and investors. Another benefit of the Xilinx development approach is fast time to market for high-capacity FPGAs at 28nm, with the expectation that a similar pattern can occur at 20nm and smaller feature dimensions. The performance and reliability levels of the SSI technology structures are comparable to integrated designs and allow a seamless interface for customers to adopt integrated products when they become cost-effective.

2011
INNOVATION

STACKED-SILICON INTERCONNECT TECHNOLOGY

Advanced Reliability Study of TSV Interposers and Interconnects

As interconnect density shrinks, and the cost of fabricating finer-pitch substrates increases, flip-chip packaging with a conventional organic buildup substrate faces a major challenge related to fine-pitch wiring. Through-silicon via (TSV) interposer technology has emerged as a good solution, providing high-wiring-density interconnection, minimizing CTE mismatch between the Cu/low-κ die and the copper-filled TSV interposer, and improving electrical performance due to shorter interconnection from the chip to the substrate.

TSV interposer wafers are manufactured by etching vias through silicon wafers and filling the vias with metal. Xilinx research indicated that the "via-first/via-middle" flow should offer the greatest interconnect density. Accordingly, TSV fabrication and assembly processes of the large logic die mounted on the TSV interposer have been optimized along with assembly on the organic substrate. Xilinx performed 3D thermal-mechanical modeling and simulation for the packaged device with TSV interposer. Devices have been subjected to thermal cycling, electromigration, and moisture-sensitivity tests. The stress of the die, low-κ layers, and fatigue life of µbumps and C4 bumps have been investigated, and Si interposer deemed a low-risk 3D path to a reliable package.

FPGA wafers are bumped to ultrafine pitch in the range of 30-60 µm using Cu pillar bump technology. The FPGA dies are diced and attached to the interposer top pads, the gap is filled, and the completed interconnect assembly is then joined to the package substrate using standard C4 flip-chip attach process flow.

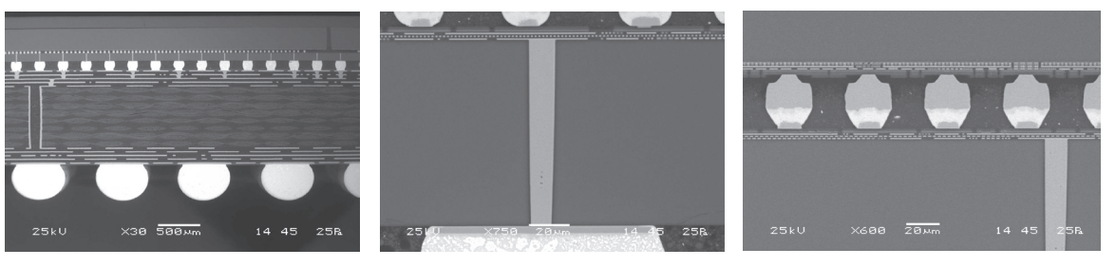


Figure 1. *Cross-sections of (a) overall assembly, (b) TSV interposer, and (c) µbumps*

Package Description

The high-performance FPGA is a four-slice 28nm chip mounted on a 25x31-mm by 100-µm-thick interposer with thousands of µbumps at 45-µm pitch. The TSV interposer is assembled on a 42.5x42.5-mm organic package with 150-µm-pitch C4 bumps, and monitored through via chains, Kelvin Structure, and daisychains (see Figure 2).

CONT'D. >>

3D Thermomechanical Simulation and Analysis

Three-dimensional models are constructed using the commercial software Abaqus to perform the package thermomechanical simulation and analysis. Then, 3D nonlinear thermomechanical global models are built focusing on warpage of the package during thermal stressing.

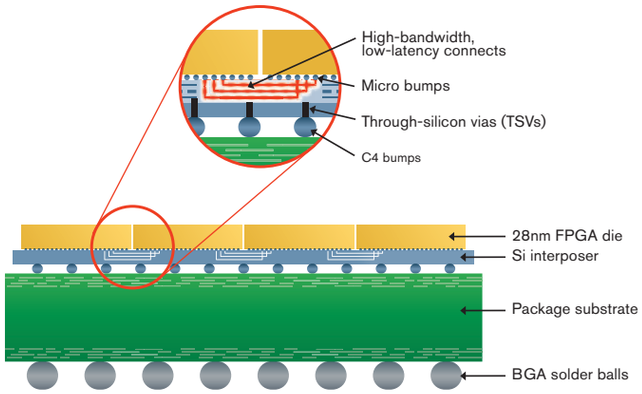


Figure 2. *Schematic of package configuration*

Xilinx studied lead-free µbumps and eutectic C4 solders in detail and a model to simulate strains, inelastic energy, and fatigue to a high level of accuracy. The results of the testing indicate that, for a given package and TSV interposer attributes and metallization, µbumps and C4 bumps undergo acceptable reliable solder inelastic strain and fatigue. This was later confirmed through reliability testing.

TSV silicon stress testing was performed in detail for reliability. Table 1 shows that the overall stresses are below fracture toughness of the materials and there seems to be no delamination or fracture risk for the interposer. This was later confirmed through reliability testing.

	MAX IN-PLANE STRESS (MPA)	MAX SHEAR STRESS (MPA)	MAX OUT-OF-PLANE STRESS (MPA)
Si	127.5	4.28	82.10
SiO2	120.3	16.47	77.06
Cu-TSV	146.3	21.75	111.3

Table 1. *TSV Silicon stresses during -55=>125C cycles*

The main focus for reliability assessment was to understand the impact of moisture and temperature cycling on the µbumps and adhesion of the underfill to the top FPGA die and thin TSV interposer substrate.

Conclusions

Xilinx studies have confirmed that the "via-first/via-middle" flow offers the greatest benefit of interconnect density. TSV processes for an aspect ratio up to 10 have been established as yielding stable, repeatable, void-free TSV vias.

Three-dimensional thermomechanical simulation models were built to study the reliability of µbumps, C4 bumps, the TSV interposer, and low-κ delamination as well as warpage. Several DOEs were performed to maximize yield and reliability. The Si interposer yielded a reliable package with acceptable warpage/coplanarity, passing 1000TCB without any crack, delamination, or void in low-κ, TSV, µbumps, and C4 bumps. Wafer-level reliability and technology assessment for SSIT were successfully completed. Volume shipments will begin in the fourth quarter of 2012.