SCALABLE, STANDARD-BASED INTERFACE FOR HIGH-SPEED TRANSMISSION AND RECEPTION OF DIGITAL VIDEO

XILINX DISPLAYPORT LOGICORE IP

Industry Demands

- Differentiated high-end display products without high NRE
- Higher image resolution, faster performance and more color depth
- Video and audio connectivity inside box, between LCDs, and across networks

The Xilinx Solution

- High-speed serial interface for professional and consumer displays
- Transmission and reception of serial digital video at up to 2.7Gbps
- Simplified design reduces EMI, lowers power and improves signal integrity
- Design to VESA DisplayPort Specification v1.1a

The Xilinx DisplayPort® LogiCORE™ IP is a high-speed serial digital video interface that replaces DVI and is an alternative to HDMI at high definition resolutions and beyond for consumer and professional displays. Target applications include HDTVs, professional broadcast monitors, digital signage, laptop and gaming LCDs, video/audio conferencing, medical and scientific imaging monitors, and command and control monitors.

The fully parameterizable core combines audio, video, and control data into packets to transmit and receive at faster speeds. Multi-lane channel support enables designers to trade off between screen resolution, pixel depth, frame rate, and additional data, such as audio. The DisplayPort LogiCORE IP uses a bidirectional 1Mbps auxiliary channel for link management and device control. The embedded clock eliminates the need for additional circuitry and makes it easier for designers to increase data rates in the future.

The DisplayPort LogiCORE IP features:

- Designed to VESA DisplayPort Specification v1.1a
- Source (Tx) and Sink (Rx) controllers perform encoding/decoding
- One or two pixel-wide main link for up to 2560x1600 monitor resolution
- Auto lane rate and width negotiation (1.6 or 2.7Gbps; 1, 2 or 4 lanes)
- HD video and optional de/interlace of secondary audio support
- 8b/10b encoding and scrambling to reduce EMI
- DisplayPort Source and Sink Reference Designs

Source and Sink Core Functional Overview

The source and sink cores perform all the required operations for the Link and Physical Layers of VESA DisplayPort v1.1a specification. They manage construction and deconstruction of video data (and optional audio data) into a standard format through the main link for transmission over high-speed serial I/O between link partners.

Main Link

The main link collects and drives data to and from the users. This interface uses horizontal and vertical sync signals for framing to match the industry standard for display controllers and easily plugs into existing video streams. Users can specify one or two pixel-wide data, number of bits per pixel, and color space.

XILINX®

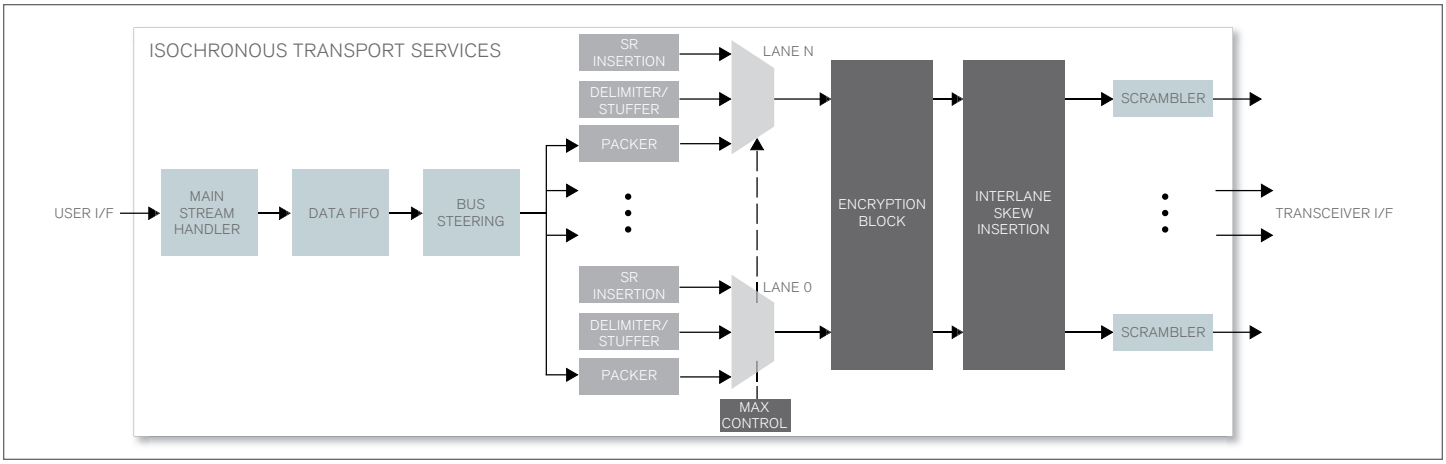
Secondary Channel

For applications requiring audio support, the source and sink cores provide an optional secondary stream interface. This I2S interface may be used to pull audio data from the main stream and on to an audio decoder that can be controlled through register access.

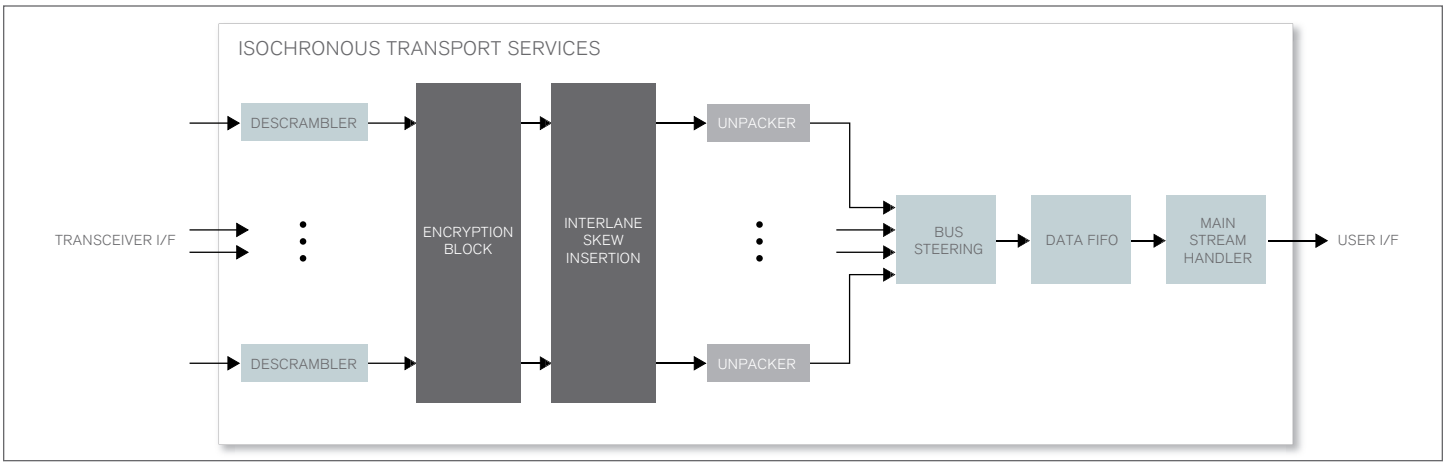
High-Speed Serial I/O

Users can specify up to 4-lane transmit and receive running at 2.7Gbps in Spartan®-6 FPGAs.

SOURCE MAIN LINK DATAPATH



SINK MAIN LINK DATAPATH



Take the NEXT STEP

For more information on available IP solutions from Xilinx, please visit **www.xilinx.com/ipcenter/index.htm**

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe
Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan
Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.
Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

Printed in the U.S.A. PN 2422-1