RELIABLE, TIME SYNCHRONIZED, LOW LATENCY, AND HIGH QUALITY OF SERVICE SOLUTION FOR REALTIME AUDIO OR VIDEO DATA.

XILINX ETHERNET AVB ENDPOINT LOGICORE IP

Industry Demands

- Guaranteed transportation of streaming audio and video on Ethernet-based networks
- Scalable open standards
- Flexibility to meet emerging specification changes

The Xilinx Solution

- Time synchronization (IEEE 802.1 AS) and traffic shaping (IEEE 802.1 Qav) to guarantee high quality of service
- Paramaterizable core, delivered through CORE Generator™ software, operating at 100 Mbps or 1Gbps based upon standard Ethernet
- Fully flexible, highly integrated system design for seamless adaptability and multiple use models

The Xilinx Ethernet Audio Video Bridging (AVB) Endpoint LogiCORE™ IP core, designed to emerging IEEE 802.1 standard from the AVB Task Group, delivers a flexible solution to enhance standard Ethernet MACs. The core provides prioritized channels through an existing MAC designed to supply a reliable, time synchronized, low latency, and high Quality of Service (QoS) solution for real-time audio or video data.

Scalable FPGA-based Solution for Multimedia-enhanced Markets

Offering portability to the high performance Xilinx Virtex®-6 FPGAs and the low cost Extended Spartan®-6 family FPGAs, the core is ideal for streaming audio and video applications for broadcast, automotive, consumer and industrial markets. This FPGA-based solution allows designers to implement an unlimited number of channels based upon available resources. The Ethernet AVB Endpoint adapts seamlessly to the Xilinx standard soft or integrated Tri-mode Ethernet MAC at 100 Mbps or 1 Gbps.

Optimal Bandwidth Preservation

Supporting data transfer for AV and legacy traffic, the core enables arbitration between data and implements bandwidth policing. This allows the user to reserve 75% of the bandwidth for AV traffic and 25% for legacy traffic thereby guaranteeing reliable data throughput.

High-Speed Processing of Timing Packets

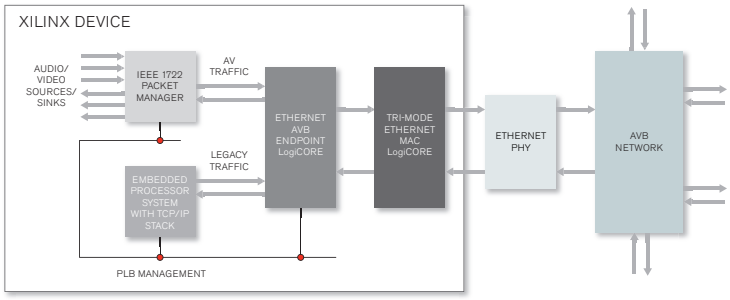
The Ethernet AVB Endpoint core and on-board 32-bit MicroBlaze™ soft processor eliminates the need for an external host processor, allowing ultra-fast processing of timing packets. The Xilinx FPGA fabric assists in hardware time-stamping of packets to eliminate operating system delays.

AVnu™

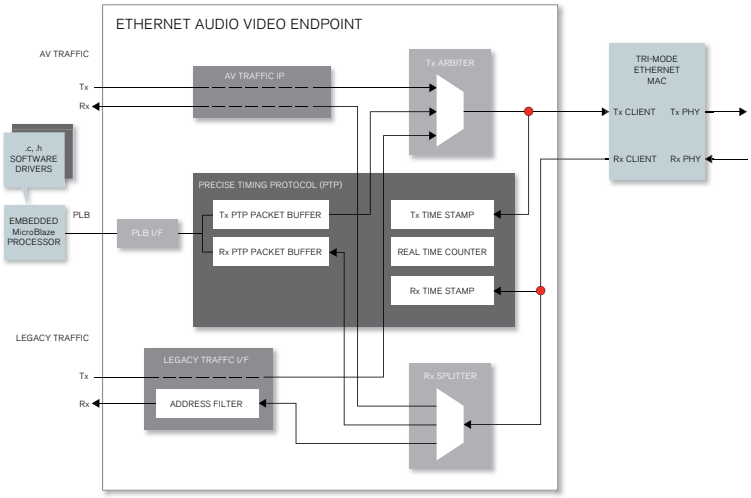
Xilinx is a founding member of the AVnu Alliance. Visit www.avnu.org for more information.

XILINX®

TYPICAL IMPLEMENTATION FOR THE ETHERNET AVB ENDPOINT CORE



FUNCTIONAL BLOCK DIAGRAM OF THE ETHERNET AVB ENDPOINT CORE



FPGA RESOURCE UTILIZATION

FPGA RESOURCE UTILIZATION			
Resources Used	LUTs	FFs	Block RAMs
Virtex-6 FPGA	1505	1829	3
Spartan-6 FPGA	1505	1829	3

Take the NEXT STEP

Visit us online at **www.xilinx.com/products/ipcenter/DO-DI-EAVB-EPT.htm**
Visit IEEE Ethernet AVB standards at **www.ieee802.org/1/pages/avbridges.html**

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Printed in the U.S.A. PN 2413