65NM PRODUCT RELIABILITY

Xilinx ships approximately 90 percent of the world's high-end FPGAs and is on track to deliver 40/45nm FPGA platforms in the first half of 2009. In keeping with that tradition and in anticipation of future customer requirements, research and development is also well underway at 32nm and below.

HTOL Test Results for 0.065 µm Si Gate CMOS Device Type XC5VxXxxx

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_A=125°C	Equivalent Device Hours at T_J=125°C	Failure Rate at 60% CL and T_J=55°C (FIT)
XC5VLX110T	3	1(1)	207	423,543	670,798	
XC5VLX30T	1	0	45	90,405	153,599	
XC5VLX50T	5	0	253	509,316	883,961	
XC5VSX50T	1	0	49	99,029	169,598	
XC5VFX70T	1	0	32	32,704	72,428	
XC5VxXxxx	11	1	586	1,154,997	1,950,379	13 FIT

Notes: 1. Failure is result of Metal 1 defect. Process improvement has been implemented.

THB Test Results for Si Gate CMOS Device Type XC5VxXxxx

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VSX50T	1	0	40	40,000
XC5VLX50T	9	0	516	520,364
XC5VxXxxx	10	0	520	523,824

TH Test Results for Si Gate CMOS Device Type XC5VxXxxx

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX50T	6	0	279	283,190

Temperature Storage Life Test Results for Si Gate CMOS Device Type XCXxXxxx

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC5VLX50	B: -55°C to +125°C	4	0	257	268,347
XC5VLX30T	B: -55°C to +125°C	1	0	20	20,520
XC5VLX50T	B: -55°C to +125°C	3	0	219	226,539
XC5VLX110T	B: -55°C to +125°C	34	0	1,299	1,334,514
XC5VLX330T	B: -55°C to +125°C	13	0	388	392,974
XC5VSX50T	B: -55°C to +125°C	4	0	264	272,964
XC5VSX95T	B: -55°C to +125°C	4	0	100	100,975
XC5VFX70T	B: -55°C to +125°C	4	0	137	138,008
XC5VFX130T	B: -55°C to +125°C	1	0	63	63,000
XC5VxXxxx	B: -55°C to +125°C	66	0	2,573	2,638,192

High-temperature Storage Life Test Results of Si Gate CMOS Device Type XC5VxXxxx

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX50T	8	0	452	462,132

CASE STUDY:

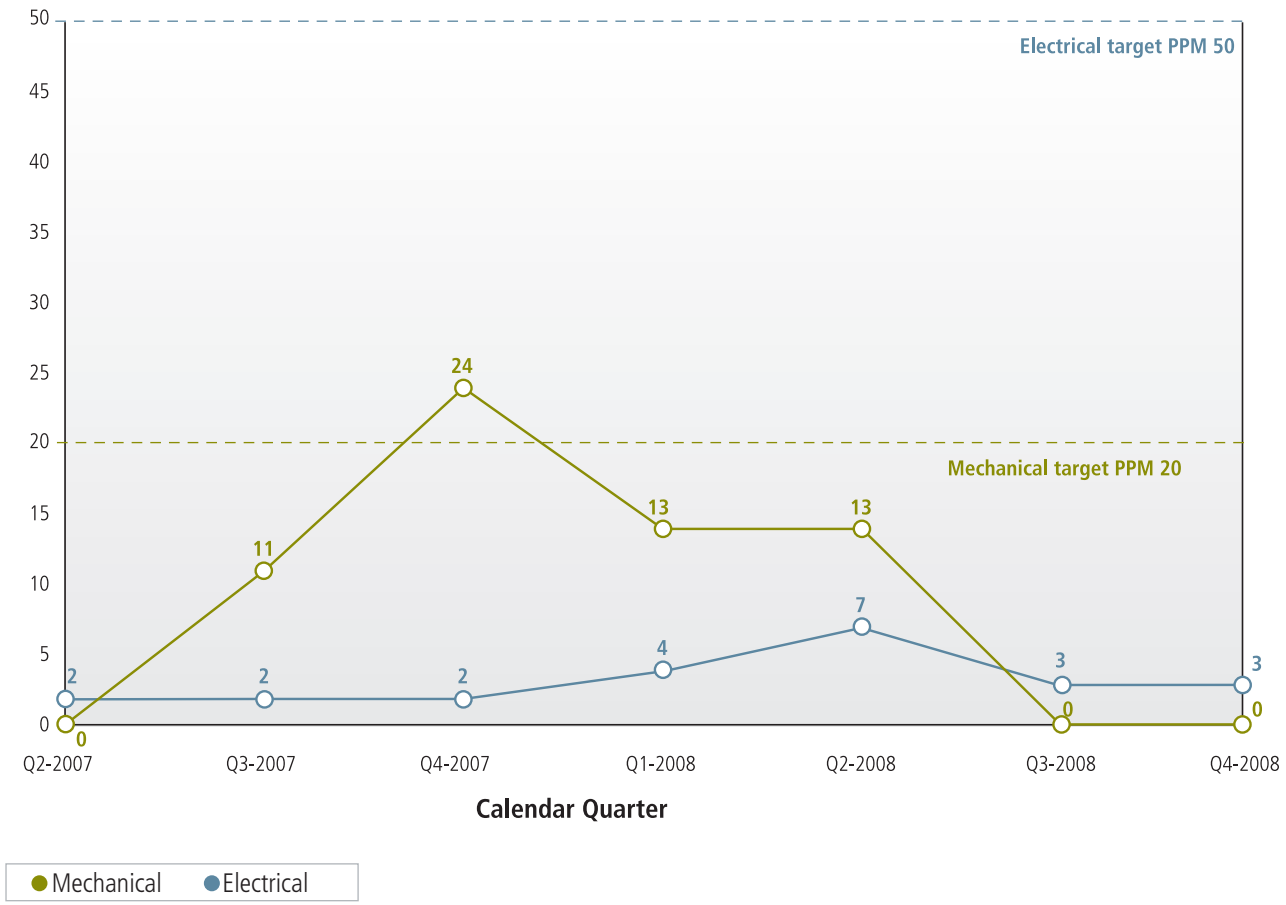
10 PPM PROJECT

Getting it Right the First Time by Striving for Zero Defects

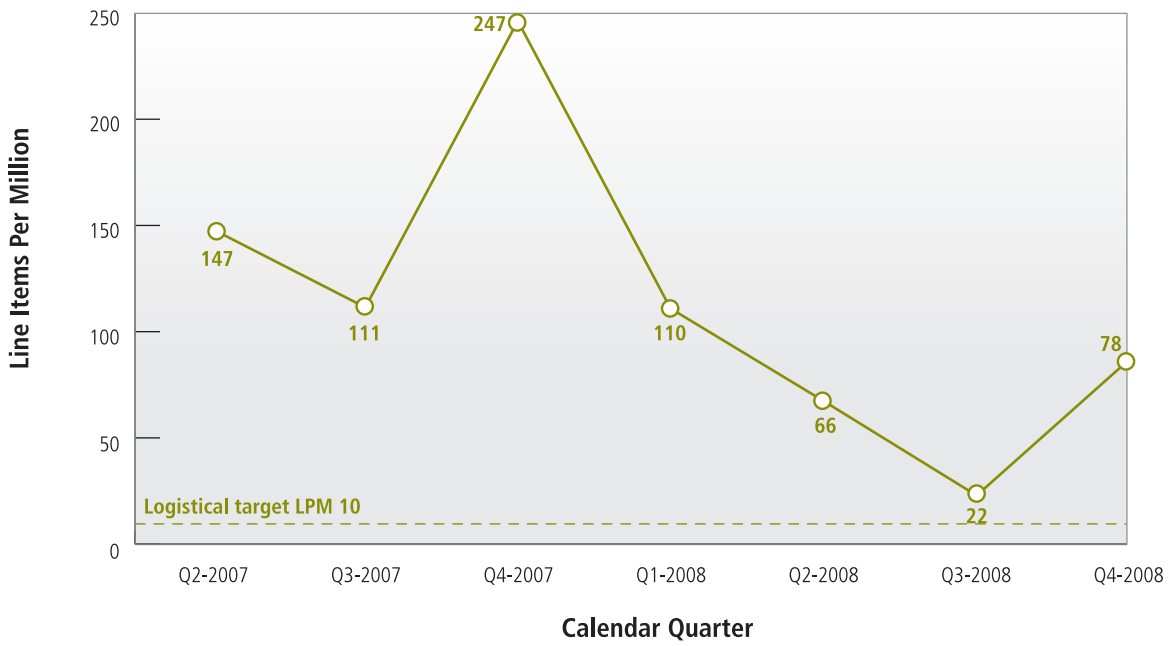
CUSTOMER PPM / LPM

Category	Q1	Q2	Q3	Q4	TARGET
Electrical	4	7	3	3	50 ppm
Mechanical	13	13	0	0	20 ppm
Logistical	110	66	22	78	20 ppm

CONFIRMED CUSTOMER EXPERIENCE (PPM) - QUARTERLY



LOGISTICAL QUALITY (LPM) - QUARTERLY



INITIATIVE GOAL:

Drive global efforts to reduce logistics quality excursions to 10 LPM level with overall goal toward zero defects

QUALITY MILESTONES	KEY RESULTS
Executed against all committed improvement actions: • Improve Logistics interim target from 70 LPM to 50 LPM • Implement FMEA continuous improvement culture	• Achieved Logistics 22 LPM versus interim goal of 50 LPM • Validated that long-term Logistical defect goal of 10 LPM is achievable: - 3 quarters @ 0 LPM in Xilinx Ireland - 1 quarter @ 0 LPM in Xilinx San Jose • 5S implementation to further drive continuous improvement culture • Every complaint investigated and understood through 8D process • Logistics FMEA completed and focused effort on longer term preventive actions • Third party and customer audits have resulted in perfect scores

QUALITY TRENDS

Xilinx pushes the boundaries of technology to raise the bar for quality and innovation. We continually develop new methods and standards that make it possible to deliver superior solutions with greater efficiency to the 20,000 customers served across diverse markets.

QUALITY FOCUS	CALENDAR YEAR 2008 RESULTS	QUALITY IMPROVEMENT FACTORS
Overall Quality	• No major customer recalls in more than three years • PPM levels achieving targets	Benefited from: - Strong Maverick controls established - Implemented spatial outlier elimination - Earlier qualification - Expanded product testing and coverage - Re-designed new products process and release criteria
Fab Quality	• 90nm defect density: 14% improvement from 2007 • 65nm defect density: 16% improvement from 2007 • Internal issues down 40% from 2006	Benefited from change control and statistical process control
Assembly Quality	• Mechanical AOQL achieved 0 PPM in the two most recent quarters (Q3 and Q4 CY08) • Internal issues down 25% from 2006	Benefited from direct material control and FMEA
Test Quality	• Electrical AOQL achieving targets: Overall = 3 PPM • Interconnect test coverage at 99% overall • Embedded IP test coverage at 98% overall • Virtex-5 platform: Interconnect and embedded IP test coverage at 99%	Benefited from DFT, BIST, software optimization for test, and process control

RELIABILITY FAILURE RATE SUMMARY

The failure rate is typically defined in FIT units. One FIT equals 1 falure per 1 billion device hours. For example, 5 failures expected out of 1 million components operating for 1000 hours will have a failure rate of 5 FIT. The following is the failure rate calculation method.

Equation 1-1

$$\text{Failure Rate} = \frac{x^2 10^9}{2(\text{No. of Devices})(\text{No. of Hours})(\text{Acc.Factor})}$$

Where:

x^2 = Chi-squared value at a desired confidence level and (2f +2) degrees of freedom, where f is the number of failures.

The acceleration factor is calculated using the Arrhenius relationship:

Equation 1-2

$$A = \exp\left\{\frac{E_a}{k\left(\frac{1}{T_{J1}} - \frac{1}{T_{J2}}\right)}\right\}$$

Where:

E_a = Thermal activation energy (0.7eV is assumed and used in failure rate calculation except EPROM in which 0.58 eV is used).

A = Acceleration factor

k = Boltzman's constant, 8.617164 x 10-5 eV/°K

T_{J1} = Use junction temperature in degrees Kelven (°K = °C +273.16)

T_{J2} = Stress junction temperature in degrees Kelvin (°K = °C +273.16)

Summary of the Failure Rates

Process Technology	Device Hours at T_J = 125°C	FIT(1)
0.065 µm	1,950,379	13
0.09 µm	8,934,645	3
0.13 µm	2,192,422	5
0.15 µm (FPGA)	3,111,774	17
0.15 µm (EPROM)	2,117,438	12
0.18 / 0.15 µm	2,544,396	10
0.18 µm	3,813,663	14
0.22 / 0.18 µm	2,034,840	13
0.22 µm	1,926,728	6
0.25 µm	3,046,159	4
0.35 µm / 0.25 µm	2,210,904	5
0.35 µm	4,518,098	15
0.35 µm (EPROM)	1,032,068	24
0.5 µm	2,113,046	12
0.6 µm	813,592	14
0.6 µm (EPROM)	1,039,921	24

Notes: 1. FIT is calculated based on an 0.7eV for EPROM, 60% C.L. and T_J of 55°C

QUALITY INDUSTRY CERTIFICATIONS

Xilinx is the:

- Only PLD supplier to achieve both TL9000 and TS16949 certifications
- First PLD supplier to achieve TL9000 certification
- First and only fabless company to achieve TS16949 certifications

XILINX FACILITY	QUALITY CERTIFICATION	CERTIFIED SINCE
San Jose, California	TL9000 / ISO 9001:2000 ISO / TS16949 2002 ISO 14001:2004 OHSAS18001	January 2004 August 2004 August 2002 October 2008
Dublin, Ireland	TL9000 / ISO 9001:2000 ISO / TS16949 2002 ISO 14001:2004 OHSAS18001	January 2004 August 2004 August 1999 October 2008
Singapore	TL9000 / ISO 9001:2000 ISO / TS16949 2002 ISO 14001:2004 OHSAS18001	January 2005 August 2005 August 2006 October 2008
Albuquerque, New Mexico	TL9000 / ISO 9001:2000 ISO / TS16949 2002	January 2005 August 2005
Denver, Colorado	ISO9001	December 2004
Hyderabad, India	TS16949	November 2008

XILINX SUPPLIERS	QUALITY CERTIFICATION	ECOSYSTEM RELATIONSHIP
UMC, Hsin-Chu, Taiwan Toshiba, Japan	TS16949:2002 ISO9001:2000	Foundry
Amkor, Korea Amkor, Phillipines STATS ChipPAC SPIL	TS16949:2002 TS16949:2002 TS16949:2002 TS16949:2002	Assembly and Test

TECHNOLOGY AND CORPORATE LEADERSHIP

Twenty-five years ago Xilinx invented the FPGA and pioneered the fabless manufacturing model. Since then, Xilinx has established a reputation as a semiconductor industry leader that consistently delivers products on cutting-edge technologies and drives innovation that sets new standards for quality.

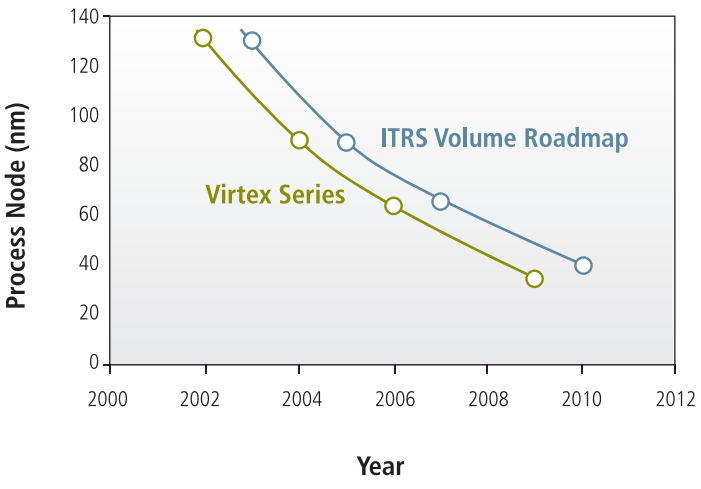
2008 INDUSTRY AWARDS	XILINX RECIPIENT	AWARD SPONSOR
Most Respected Public Fabless Company	Xilinx Corporate	Global Semiconductor Alliance (third award in last seven years)
ALICE Industrial Collaboration	Xilinx Corporate	CERN
100 Best Corporate Citizens	Xilinx Corporate	CRO Magazine
Best Product of the Year	Virtex-5 FXT FPGA	EDN China
Leading Product of the Year	ISE 10.1 Design Tools	EDN China
Top 10 China Influential Embedded System Finalist	Virtex-5 FXT FPGA MicroBlaze v7 Processor AccelDSP and System Generator for DSP Tools	EEPW China
Editor's Choice Award	Spartan-3A FPGA	Portable Design Magazine
2007 INDUSTRY AWARDS	**XILINX RECIPIENT**	**AWARD SPONSOR**
Influential Embedded System New Technology Award	Spartan-3A DSP FPGA	EEPW China
Top 10 China Influential Embedded System	Virtex-5 FPGAs	EEPW China
Digital IC Product of the Year	Virtex-5 LXT FPGAs	EDN China
Semiconductor Product of Year	Virtex-5 LXT FPGA Platform	Elektra Awards
Hot 100 Products	Spartan-3AN FPGA Platform	EDN Magazine
Best of 2007 EDA/FPGA Tool	ISE 9.1i Design Tools	Electronic Design Magazine
Green Mark Platinum Award	Xilinx Asia-Pacific HQ	Singapore Ministry of National Development
LEED Green Building Certification	Xilinx North America HQ	US Green Building Council
Design Vision Award	PlanAhead™ 8.2 Software	IEC
Product & Innovation of the Year	Virtex-5 FPGA	EDN Magazine
Design Team of the Year	Virtex-5 FPGA Design Team	EDN Magazine
Product of the Year	Virtex-5 FPGA	EE Times China
Company of the Year Finalist	Xilinx Corporate	EE Times China
Ultimate Product Finalist	Virtex-5 FPGA PlanAhead 8.2 Software	EE Times ACE Awards
Most Innovative Product of Year	Virtex-5 FPGA	Electronique Magazine
100 Best Corporate Citizens for	Xilinx Corporate	CRO/Business Ethics Magazine

CASE STUDY:

VIRTEX-5 FPGA NEW PRODUCT EVALUATION

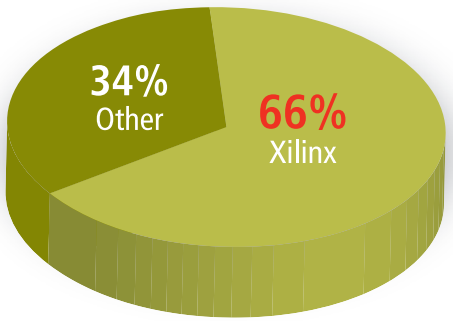
Technology Innovation Leads to Market Share Leadership

ITRS and Virtex Products



* International Technology Roadmap for Semiconductors 2001-2007

Total High-End FPGA Market Share 2001-2007



INITIATIVE GOAL:

Establish process stability and manufacturing readiness

QUALITY MILESTONES

Virtex-5 LX and LXT FPGA platforms were first products put through NPE and NPI process

- Performed extensive design validation and characterization
- Started early qualification evaluations
- Stronger release criteria for engineering samples and production conversions

Significantly increased overall coverage as compared to previous generation products

KEY RESULTS

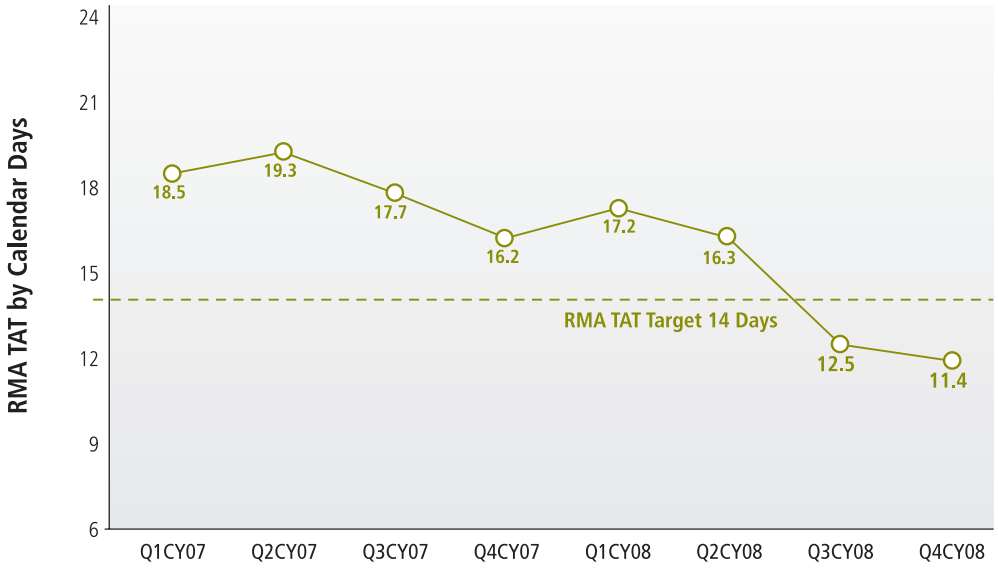
- Dual source with fabrication process and materials from both foundries included in the evaluation
- Reliability of UMC 65nm process achieved world-class minimum failure rates.
  - Virtex-5 devices achieved 14.6 FIT* for HTOL, a score that rivals many mature processes
- Expanded voltage and temperature ranges beyond datasheet specifications to ensure sufficient margin for functional operation
  - Calibrated to industrial grade range to provide further assurance of safe and comfortable operating margin
- Expanded number and type of tests to ensure product feature coverage
  - Virtex-5 FPGA 383,418,575 measurements vs. Virtex-4 FPGA 100,680,000 measurements
  - Nearly 400% increase in coverage
- Met delivery commitments
  - 100% on time for production release (new product)
  - 95%+ on time delivery to factory schedule dates

*See Xilinx Reliability Report for current FIT rate.

CASE STUDY:

STREAMLINING THE RETURNS PROCESS

Global Infrastructure, Regional Support



INITIATIVE GOAL:

Improve customer product returns process worldwide

QUALITY MILESTONES

Launched new online RMA web portal

Established two new engineering labs:

- Product Quality Engineering (PQE) Lab for RMA fault isolation
- Device Analysis Lab (DAL) for physical failure analysis

Expanded RMA regional support in Xilinx Singapore headquarters

Deployed FPGA best practices training to customers for improved designs and fewer manufacturing delays.

KEY RESULTS

- Reduced overall factory average RMA cycle time to 11.4 calendar days
- Customer-oriented approach allows transparent view into Xilinx processes:
  - Direct case initiation for quickly opening new cases
  - 24/7 status for in-process cases
  - Improved communication through real-time notifications and updates
- 28% of global RMA activities in Sep 2008 supported in Singapore
  - Increase to 50% in January 2009, 3 months ahead of schedule
- System designers empowered to perform quality control through more rigorous design and production release reviews
- More robust FPGA designs for customers and fewer production issues and product returns
- Best practices checklist: http://www.xilinx.com/products/quality/fpga_best_practices.htm

XILINX QUALITY RESOURCE GUIDE

Xilinx publishes a comprehensive range of information about its global quality programs, metrics, and documentation. This table provides an overview of the detailed reports accessible to Xilinx customers either by request or online, as well as direct links to Xilinx training and support sites.

Please visit the Xilinx Quality home page at: http://www.xilinx.com/products/quality/index.htm

REPORT TITLE	REPORT AVAILABILITY
Quality Policy	http://www.xilinx.com/products/quality/Xilinx_Quality_Policy.pdf
Xilinx Quality Manual	http://www.xilinx.com/products/quality/QualityManual.pdf
Quality Certifications	See links to documentation for each of the following certifications at: http://www.xilinx.com/products/quality/index.htm ISO 9001:2000 / TL 9000 (XSJ, XAQ, XIR, XAP) ISO 9001:2000 (XCO) ISO/TS 16949:2002 (XSJ) ISO/TS 16949:2002 (XAQ) ISO/TS 16949:2002 (XIR) ISO/TS 16949:2002 (XAP) QML per MIL-PRF-38535 ISO 14001:2004 (XSJ) ISO 14001:2004 (XIR) ISO 14001:2004 (XAP) OHSAS 18001:2007 (XIR, XSJ, XAP) MIL-PRF-38535
Device Reliability Report (quarterly)	http://www.xilinx.com/support/documentation/user_guides/ug116.pdf
Product Characterization Reports	Available on request
Silicon Stepping	http://www.xilinx.com/products/quality/silicon-stepping.htm
RoHS and Pb-Free Compliance	http://www.xilinx.com/support/mysupport.htm
Supplier Management	http://www.xilinx.com/products/quality/submgmt.htm
Product Change Notifications	http://www.xilinx.com/support/documentation/customer_notices.htm
RMA and Returns Instructions	http://www.xilinx.com/products/quality/rma.htm
FPGA Design Best Practices	http://www.xilinx.com/products/quality/fpga_best_practices.htm
Training	http://www.xilinx.com/support/education-home.htm
Xilinx Support Home Page	http://www.xilinx.com/support/mysupport.htm
Contact Us	http://www.xilinx.com/company/contact.htm