

## Spartan-3AN Platform

### Non-volatile

Part Number		XC3S50AN	XC3S200AN	XC3S400AN	XC3S700AN	XC3S1400AN
Logic Resources	System Gates <sup>(1)</sup>	50K	250K	400K	700K	1400K
	Slices <sup>(2)</sup>	704	1,792	3,584	5,888	11,264
	Logic Cells	1,584	4,032	8,064	13,248	25,344
	CLB Flip-Flops	1,408	3,584	7,168	11,776	22,528
Memory Resources	Maximum Distributed RAM (Kbits)	11	28	56	92	176
	Block RAM Blocks	3	16	20	20	32
	Total Block RAM (Kbits)	54	288	360	360	576
	User Flash (Kbits) <sup>(3)</sup>	627	3,054	2,380	5,779	12,251
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	8	8
I/O Resources	Maximum Single Ended I/Os	108	195	311	372	502
	Maximum Differential I/O Pairs	50	90	142	165	227
	I/O Standards Supported	LVTTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25 & 33, LVPECL25 & 33, Mini-LVDS25 & 33, RSDS25 & 33, TMDS33, PPDS25 & 33				
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	—
	Dedicated Multipliers	3	16	20	20	32
	Device DNA Security	Yes	Yes	Yes	Yes	Yes
Speed Grades	Commercial	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5
	Industrial	-4	-4	-4	-4	-4
Configuration	Configuration Memory Bits (Kbits)	0.4 <sup>(6)</sup>	1.2 <sup>(6)</sup>	1.9 <sup>(6)</sup>	2.7 <sup>(6)</sup>	4.8 <sup>(6)</sup>
Package <sup>(7)</sup> Area		Maximum User I/Os				
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)						
VQ100	16 x 16 mm					
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)						
TQ144	22 x 22 mm	108				
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)						
FT256	17 x 17 mm		195			
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)						
CS484	19 x 19 mm					
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)						
FG320	19 x 19 mm					
FG400	21 x 21 mm			311		
FG484	23 x 23 mm				372	
FG676	27 x 27 mm					502

- Notes: 1. System Gates include 20%-30% of CLBs used as RAMs 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.  
3. User Flash is the space left in the on-chip Flash after a portion is used to store configuration bitstream.  
4. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).  
5. The Low-power option is exclusively available in CS(G)484 package and Industrial temperature range.  
6. Spartan-3AN can be configured using on-chip Flash. 7. All products available Pb-free and RoHS-Compliant.