



Spartan-6 LXT FPGAs

Optimized for Low Cost Logic, DSP, and Memory
with High-speed Serial Connectivity (1.2 Volt)

	Part Number	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Logic Resources	Slices ⁽¹⁾	3,758	6,822	11,662	15,822	23,038
	Logic Cells ⁽²⁾	24,051	43,661	74,637	101,261	147,443
	CLB Flip-Flops	30,064	54,576	93,296	126,576	184,304
Memory Resources	Maximum Distributed RAM (Kbits)	229	401	692	976	1,355
	Block RAM (18K bits each)	52	116	172	268	268
	Total Block RAM (Kbits) ⁽³⁾	936	2,088	3,096	4,824	4,824
Clock Resources	Clock Manager Tiles (CMT) ⁽⁴⁾	2	4	6	6	6
I/O Resources	Maximum Single-Ended Pins	250	296	348	498	540
	Maximum Differential Pairs	125	148	174	249	270
Embedded Hard IP Resources	DSP48A1 Slices ⁽⁵⁾	38	58	132	180	180
	PCI Express® Endpoint Block	1	1	1	1	1
	Memory Controller Blocks	2	2	4	4	4
	GTP Low-Power Transceivers	2	4	8	8	8
Speed Grades	Commercial	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4
	Industrial	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3
Configuration	Configuration Memory (Mbits)	4.4	77	19.6	17.1	28.0
	Package	Area	Maximum User I/O: SelectIO™ Interface Pins (GTP Transceivers) ⁽⁷⁾			
Chip Scale Packages (CPG): Pb-free wire-bond BGA (0.5 mm ball spacing)						
	CPG196	8 x 8 mm				
TQFP Packages (TQG): Pb-free thin QFP (0.5 mm lead spacing)						
	TQG144	20 x 20 mm				
Chip Scale Packages (CSG): Pb-free wire-bond chip scale BGA (0.8 mm ball spacing)						
	CSG225	13 x 13 mm				
	CSG324	15 x 15 mm	190 (2)	190 (4)		
	CSG484	19 x 19 mm		296 (4)	292 (4)	296 (4)
FGA Packages (FTG): Pb and Pb-free wire-bond fine-pitch thin BGA (1.0 mm ball spacing)						
	FT(G)256	17 x 17 mm				
FGA Packages (FGG): Pb and Pb-free wire-bond fine-pitch BGA (1.0 mm ball spacing)						
	FG(G)484	23 x 23 mm	250 (2)	296 (4)	268 (4)	296 (4)
	FG(G)676	27 x 27 mm		348 (8)	376 (8)	396 (8)
	FG(G)900	31 x 31 mm			498 (8)	540 (8)

- Notes:
- Each Spartan-6 FPGA CLB contains four LUTs and eight flip-flops.
 - Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
 - Block RAMs are fundamentally 18Kb in size. Each block can also be used as two independent 9Kb blocks.
 - Each CMT contains two DCMs and one PLL.
 - Each DSP48A1 slice contains an 18x18 multiplier, an adder and an accumulator.
 - Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.
 - Due to the transceivers in the LXT devices, the LX pinouts are not compatible with the LX device pinouts.