

## Virtex-5 FXT FPGA Platform

Optimized for Embedded Processing with High-Speed Serial Connectivity (1.0 Volt)

		Part Number	XC5VFX30T	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T
		EasyPath™ Cost Reduction Solutions <sup>(1)</sup>	—	XCE5VFXT70T	XCE5VFXT100T	XCE5VFXT130T	XCE5VFXT200T
Logic Resources	Slices <sup>(2)</sup>	5,120	11,200	16,000	20,480	30,720	
	Logic Cells <sup>(3)</sup>	32,768	71,680	102,400	131,072	196,608	
	CLB Flip-Flops	20,480	44,800	64,000	81,920	122,880	
Memory Resources	Maximum Distributed RAM (Kbits)	380	820	1,240	1,580	2,280	
	Block RAM/FIFO w/ECC (36Kbits each)	68	148	228	298	456	
	Total Block RAM (Kbits)	2,448	5,328	8,208	10,728	16,416	
Clock Resources	Digital Clock Managers (DCM)	4	12	12	12	12	
	Phase Locked Loop (PLL)/PMCD	2	6	6	6	6	
I/O Resources <sup>(4)</sup>	Maximum Single-Ended Pins	360	640	680	840	960	
	Maximum Differential I/O Pairs	180	320	340	420	480	
	I/O Standards	HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II					
Embedded <sup>(5)</sup> Hard IP Resources	DSP48E Slices	64	128	256	320	384	
	PowerPC® 440 Processor Blocks	1	1	2	2	2	
	PCI Express Endpoint Blocks	1	3	3	3	4	
	10/100/1000 Ethernet MAC Blocks	4	4	4	6	8	
	RocketIO™ GTP Low-Power Transceivers	—	—	—	—	—	
	RocketIO™ GTX High-Speed Transceivers	8	16	16	20	24	
Speed Grades	Commercial	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1	
Configuration	Configuration Memory (Mbits)	13.6	27.1	39.4	49.3	70.9	
Package <sup>(6,7)</sup>		Area	Available User I/Os				
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)							
FF665		27 x 27mm	360 (8)	360 (8)			
FF1136		35 x 35mm		640 (16)	640 (16)		
FF1738		42.5 x 42.5mm			680 (16)	840 (20) 960 (24)	

- Notes:
- EasyPath™ solutions provide a conversion-free path for volume production.
  - A single Virtex-5 CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
  - Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
  - Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
  - One system monitor block included in all devices.
  - Available I/O for each device-package combination: number of SelectIO pins (number of RocketIO transceivers).
  - All products available Pb-free and RoHS-Compliant.