

## Virtex-5 SXT FPGA Platform Optimized for DSP with Low-power Serial Connectivity (1.0 Volt)

	Part Number	XC5VSX35T	XC5VSX50T	XC5VSX95T	XC5VSX240T
	EasyPath™ Cost Reduction Solutions <sup>(1)</sup>	—	XCE5VSX50T	XCE5VSX95T	XCE5VSX240T
Logic Resources	Slices <sup>(2)</sup>	5,440	8,160	14,720	37,440
	Logic Cells <sup>(3)</sup>	34,816	52,224	94,208	239,616
	CLB Flip-Flops	21,760	32,640	58,880	149,760
Memory Resources	Maximum Distributed RAM (Kbits)	520	780	1,520	4,200
	Block RAM/FIFO w/ECC (36Kbits each)	84	132	244	516
	Total Block RAM (Kbits)	3,024	4,752	8,784	18,576
Clock Resources	Digital Clock Managers (DCM)	4	12	12	12
	Phase Locked Loop (PLL)/PMCD	2	6	6	6
I/O Resources <sup>(4)</sup>	Maximum Single-Ended Pins	360	480	640	960
	Maximum Differential I/O Pairs	180	240	320	480
	I/O Standards	HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II			
Embedded <sup>(5)</sup> Hard IP Resources	DSP48E Slices	192	288	640	1,056
	PowerPC® 440 Processor Blocks	—	—	—	—
	PCI Express Endpoint Blocks	1	1	1	1
	10/100/1000 Ethernet MAC Blocks	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers	8	12	16	24
	RocketIO™ GTX High-Speed Transceivers	—	—	—	—
Speed Grades	Commercial	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2
	Industrial	-1, -2	-1, -2	-1, -2	-1
Configuration	Configuration Memory (Mbits)	13.4	20.0	35.8	79.7
	Package <sup>(6,7)</sup>	Area	Available User I/Os		
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)					
	FF665	27 x 27mm	360 (8)	360 (8)	
	FF1136	35 x 35mm		480 (12)	640 (16)
	FF1738	42.5 x 42.5mm			960 (24)

- Notes:
1. EasyPath™ solutions provide a conversion-free path for volume production.
  2. A single Virtex-5 CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
  3. Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
  4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
  5. One system monitor block included in all devices.
  6. Available I/O for each device-package combination: number of SelectIO pins (number of RocketIO transceivers).
  7. All products available Pb-free and RoHS-Compliant.