

		<b>Virtex-5 TXT Platform Optimized for Ultra-High Bandwidth</b>	
		<b>XC5VTX150T</b>	<b>XC5VTX240T</b>
		Part Number	
		EasyPath™ Cost Reduction Solutions <sup>(1)</sup>	XCE5VTXT150T XCE5VTXT240T
Logic Resources	Slices <sup>(2)</sup>	23,200	37,440
	Logic Cells <sup>(3)</sup>	148,480	239,616
	CLB Flip-Flops	92,800	149,760
Memory Resources	Maximum Distributed RAM (Kbits)	1,500	2,400
	Block RAM/FIFO w/ECC (36Kbits each)	228	324
	Total Block RAM (Kbits)	8,208	11,664
Clock Resources	Digital Clock Managers (DCM)	12	12
	Phase Locked Loop (PLL)/PMCD	6	6
I/O Resources <sup>(4)</sup>	Maximum Single-Ended Pins	680	680
	Maximum Differential I/O Pairs	340	340
	I/O Standards	HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II	
Embedded <sup>(5)</sup> Hard IP Resources	DSP48E Slices	80	96
	PowerPC® 440 Processor Blocks	—	—
	PCI Express Endpoint Blocks	1	1
	10/100/1000 Ethernet MAC Blocks	4	4
	RocketIO™ GTP Low-Power Transceivers	—	—
	RocketIO™ GTX High-Speed Transceivers	40	48
Speed Grades	Commercial	-1, -2	-1, -2
	Industrial	-1, -2	-1, -2
Configuration	Configuration Memory (Mbits)	43.4	65.8
		<b>Package <sup>(6,7)</sup></b>	<b>Area</b>
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)			
	FF324	19 x 19mm	
	FF676	27 x 27mm	
	FF1153	35 x 35mm	
	FF1760	42.5 x 42.5mm	
	FF323	19 x 19mm	
	FF665	27 x 27mm	
	FF1136	35 x 35mm	
	FF1156	35 x 35mm	360 (40)
	FF1738	42.5 x 42.5mm	
	FF1759	42.5 x 42.5mm	680 (40) 680 (48)

- Notes:
1. EasyPath™ solutions provide a conversion-free and low risk path for volume production.
  2. A single Virtex-5 CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
  3. Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
  4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
  5. One system monitor block included in all devices.
  6. Available I/O for each device-package combination: number of SelectIO pins (number of RocketIO transceivers).
  7. All products available Pb-free and RoHS-Compliant.