



Virtext-6 HXT FPGAs

Optimized for Communications Systems Requiring Highest-bandwidth Serial Connectivity (1.0 Volt)

Part Number		XC6VHX250T	XC6VHX255T	XC6VHX380T	XC6VHX565T
EasyPath™ FPGA Cost Reduction Solutions ⁽¹⁾		XC6VHX250T	XC6VHX255T	XC6VHX380T	XC6VHX565T
Logic Resources	Slices ⁽²⁾	39,360	39,600	59,760	88,560
	Logic Cells ⁽⁸⁾	251,904	253,440	382,464	566,784
	CLB Flip-Flops	314,880	316,800	478,080	708,480
Memory Resources	Maximum Distributed RAM (Kbits)	3,040	3,050	4,570	6,360
	Block RAM/FIFO w/ ECC (36Kbits each)	504	516	768	912
	Total Block RAM (Kbits)	18,144	18,567	27,648	32,832
Clock Resources	Mixed Mode Clock Managers (MMCM)	12	12	18	18
I/O Resources ^(4, 5)	Maximum Single-Ended I/O	320	480	720	720
	Maximum Differential I/O Pairs	160	240	360	360
Embedded Hard IP Resources ⁽⁶⁾	DSP48E1 Slices	576	576	864	864
	PCI Express® Interface Blocks	4	2	4	4
	10/100/1000 Ethernet MAC Blocks	4	2	4	4
	GTX Low-Power Transceivers	48	24	48	48
	GTH High-Speed Transceivers	–	24	24	24
Speed Grades	Commercial	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2
	Industrial	-1, -2	-1, -2	-1, -2	-1
Configuration	Configuration Memory (Mbits)	76.2	76.2	114.2	153.2
Package ⁽⁷⁾	Area	Available User I/O: SelectIO Pins ^(4, 5) (GTX Low-power Transceivers, GTH High-speed Transceivers)			
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)					
FF1154	35 x 35 mm	320 (48, 0)		320 (48, 0)	
FF1155	35 x 35 mm		440 (24, 12)	440 (24, 12)	
FF1923	45 x 45 mm		480 (24, 24)	720 (40, 24)	720 (40, 24)
FF1924	45 x 45 mm			640 (48, 24)	640 (48, 24)

- Notes:
1. EasyPath™ solutions provide a conversion-free, low-risk path for volume production.
 2. A single Virtext-6 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops (twice the number found in a Virtext-4 FPGA slice), for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
 3. Virtext-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
 4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 5. I/O standards supported: HT, LVCMOS (2.5V, 1.8V, 1.5V, 1.2V), HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), SSTL (1.5V).
 6. One system monitor block included in all devices.
 7. All products available Pb-free and RoHS-Compliant (FFG).
 8. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.