



Virtex-6 SXT FPGAs
 Optimized for Ultra
 High-performance DSP with
 Low-power Serial Connectivity
 (1.0 Volt, 0.9 Volt)

	Part Number	XC6VVSX315T	XC6VVSX475T
	EasyPath™ FPGA Cost Reduction Solutions ⁽¹⁾	XCE6VVSX315T	XCE6VVSX475T
Logic Resources	Slices ⁽²⁾	49,200	74,400
	Logic Cells ⁽³⁾	314,880	476,160
	CLB Flip-Flops	393,600	595,200
Memory Resources	Maximum Distributed RAM (Kbits)	5,090	7,640
	Block RAM/FIFO w/ ECC (36Kbits each)	704	1,064
	Total Block RAM (Kbits)	25,344	38,304
Clock Resources	Mixed Mode Clock Managers (MMCM)	12	18
I/O Resources ^(4, 5)	Maximum Single-Ended I/O	720	840
	Maximum Differential I/O Pairs	360	420
Embedded Hard IP Resources ⁽⁶⁾	DSP48E1 Slices	1,344	2,016
	PCI Express® Interface Blocks	2	2
	10/100/1000 Ethernet MAC Blocks	4	4
	GTX Low-Power Transceivers	24	36
	GTH High-Speed Transceivers	–	–
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2
	Industrial	-L1, -1, -2	-L1, -1
Configuration	Configuration Memory (Mbits)	99.6	149.4
	Package ⁽⁷⁾	Area	Available User I/O: SelectIO Pins ^(4, 5) (GTX Low-power Transceivers, GTH High-speed Transceivers)
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)			
	FF484	23 x 23 mm	
	FF784	29 x 29 mm	
	FF1156	35 x 35 mm	600 (20, 0) 600 (20, 0)
	FF1759	42.5 x 42.5 mm	720 (24, 0) 840 (36, 0)
	FF1760	42.5 x 42.5 mm	

- Notes:
1. EasyPath™ solutions provide a conversion-free, low-risk path for volume production.
 2. A single Virtex-6 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
 3. Virtex-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
 4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 5. I/O standards supported: HT, LVCMOS (2.5V, 1.8V, 1.5V, 1.2V), HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), SSTL (1.5V).
 6. One system monitor block included in all devices.
 7. All products available Pb-free and RoHS-Compliant (FFG).
 8. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.