		Spartan-3A DSP	
	Part Number	XA3SD1800A	XA3SD3400A
Logic Resources	System Gates (1)	1800K	3400K
	Slices (2)	16,640	23,872
	Logic Cells	37,440	53,712
	CLB Flip-Flops	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kbits)	260	373
	Block RAM Blocks	84	126
	Total Block RAM (Kbits)	1,512	2,268
Clock Resources	Digital Clock Managers (DCMs) – S3/DLLs – SIIE	8	8
I/O Resources	Maximum Single Ended I/Os	519	469
	Maximum Differential I/O Pairs	227	213
	I/O Standards Supported		
Embedded Hard IP Resources	DSP48A Slices	84	126
	Dedicated Multipliers	84 (3)	126 (3)
	Device DNA Security	Yes	Yes
Miscellaneous	Temperature Range (4)	I, Q	I
	Speed Grade	-4	-4
	RoHS (Pb-free)	Yes	Yes
	XA Released	Yes	Yes
Configuration	Configuration Memory Bits (Mbits)	8.2	11.7

Package	Area	Maximum User I/Os	
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)			
VQG100	16 x 16 mm		
Chip Scale Packages (CP): wire-bond chip-scale BGA (0.5 mm ball spacing)			
CPG132	8 x 8 mm		
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)			
TQG144 (5)	22 x 22 mm		
PQFP Packages (PQ): wire-bond plastic QFP (0.5 mm lead spacing)			
PQG208	30.6 x 30.6 mm		
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)			
FTG256 (5)	17 x 17 mm		
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)			
CSG484	19 x 19 mm	309	309
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)			
FGG400	21 x 21 mm		
FGG456	23 x 23 mm		
FGG484	23 x 23 mm		
FGG676	27 x 27 mm	519	469

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
4. Temperature Range Automotive I (T_j = -40°C to +100°C); Automotive Q (T_j = -40°C to +125°C). 5. Spartan-IIE is not offered in "G" (Pb-free) packages.