INDUSTRY'S ONLY TRIPLE MODULAR REDUNDANCY DEVELOPMENT TOOL FOR RE-CONFIGURABLE FPGAS

XILINX TMRTOOL

Challenge for Designing Circuits with Triple Modular Redundancy (TMR)

- Mastering and implementing TMR into a design greatly increases the complexity and the time it takes to build and debug a system

The Xilinx TMRTool Solution

- Works seamlessly with any HDL and Synthesis tool to automatically build triple modular redundancy into a Xilinx FPGA-based design
- Accelerates design cycle by allowing designers to devote more time to system design and debugging, and less time to the complex details of TMR

The Xilinx TMR methodology, along with scrubbing, provides full single-event upset (SEU) and single-event transient (SET) immunity for any Virtex® FPGA design. In addition, the TMRTool:

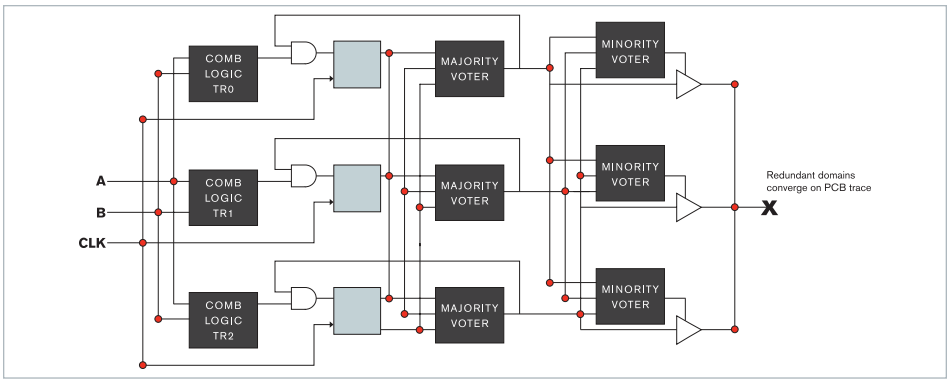
- Supports Windows 2000/XP with ISE™ 6.3i, 7.1i, 8.2i and 9.2i tools, all design entry methods, HDL, and synthesis tools
- Provides optional SRL16 extraction and optional half-latch extraction capability
- Increases productivity by reducing errors, speeding TMR implementation, and enabling easy integration of custom-built TMR modules while giving designers complete control over how their design is triplicated

Xilinx Triple Modular Redundancy Technology

Traditional TMR does not protect against SEUs in voting logic or against SETs, and does not lend itself well to the re-configurability of Xilinx FPGAs. Unlike traditional TMR, the Xilinx TMR approach involves:

- Triplicating all inputs including clocks and throughput (combinational) logic
- Triplicating feedback logic and inserting majority voters on feedback paths
- Triplicating all outputs, using minority voters to detect and disable incorrect output paths

AUTOMATIC IMPLEMENTATION OF TRIPLE REDUNDANCY FOR SEU MITIGATION



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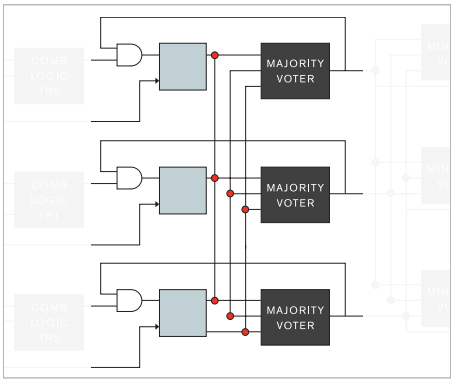
Xilinx TMR State Machines

Finite State Machines pose a special problem for TMR in re-programmable devices. To operate continuously in the presence of SEUs, each redundant state machine domain must remain synchronized with the others. For traditional TMR, this means that state machines have to be reset to fully recover from a SEU. Xilinx TMR solves this problem by inserting voters on all feedback paths, so that redundant state machines are continually synchronized with each other - eliminating the need for resets to recover from SEUs.



TMRTool automatically implements Xilinx TMR methodology for state machines.

Protection from SEUs in Voting Circuits

The major difference between traditional TMR approaches and the Xilinx TMR approach: voters themselves are triplicated, as well as redundant domains coverage on the printed circuit board. If an upset occurs in throughput logic or in a state machine somewhere in the design, one of the redundant design domains will behave differently from the others. The output voter for that domain will detect that its domain is behaving differently and disable the three-state buffer for that domain, placing its pin in a high impedance state. The other two domains will continue to operate correctly, driving the correct output off the chip. If a voter is upset, the worst it can do is disable the output of a domain that is behaving correctly. As with the first scenario, the other domains will continue to operate correctly, driving the correct output off the chip.

Take the NEXT STEP

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