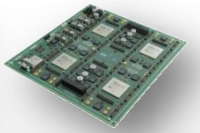
Xilinx 7 Series FPGA Power Benchmark Design Summary

June 2014

Application-centric Benchmarking Process


100G Packet Processor


OTN Muxponder


ASIC Emulation


Wireless Radio & Satellite Modem


Edge QAM


AVB Switcher


Military Radio

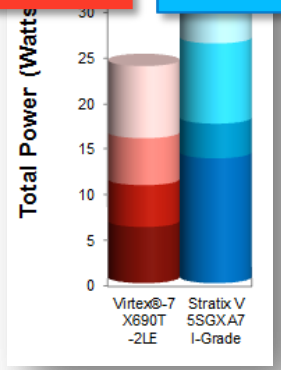

Mobil Backhaul

FPGA resource counts, toggle rates, clock speeds…

- Xilinx Power Estimator (XPE) version 2014.2
- MAX condition used to estimate worst-case static power

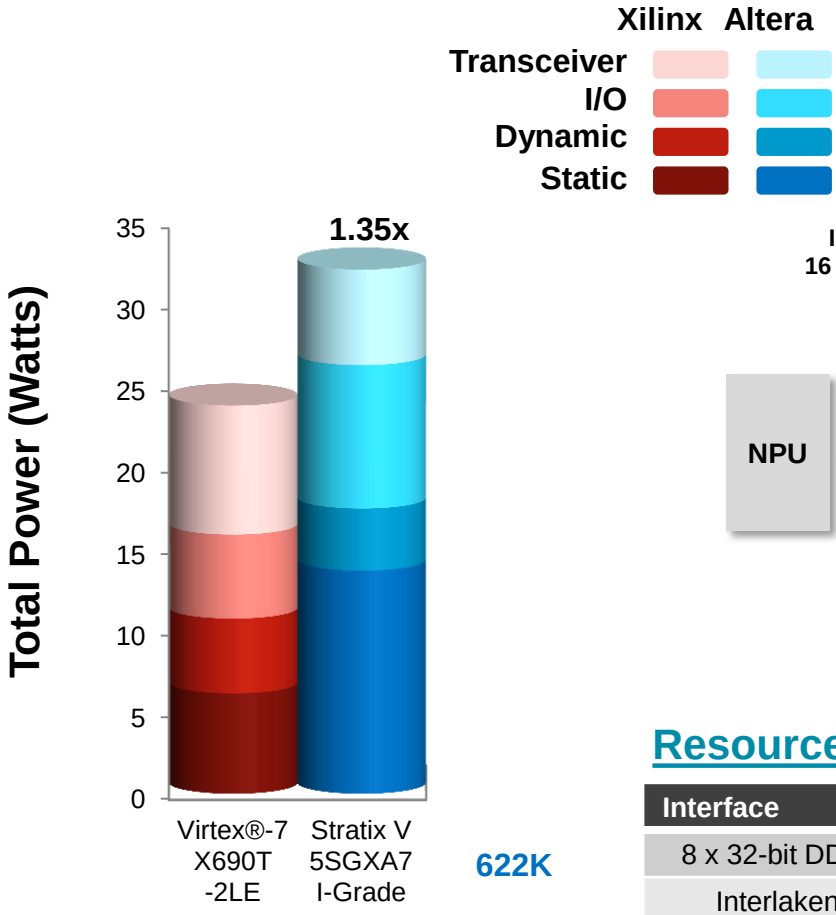
XPE

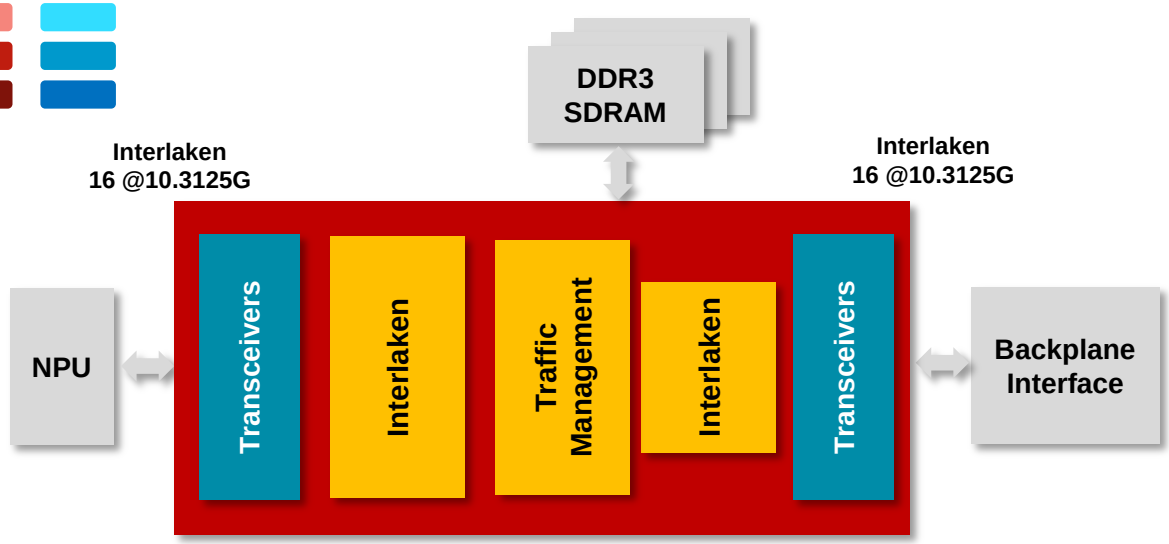
Competitor's Estimator



- Early Power Estimator (EPE) versions 14.0
- MAX condition used to estimate worst-case static power

Power Benchmark: Traffic Manager in 100G Line Card Virtex-7 X690T FPGA





Resources

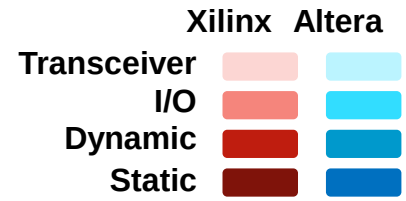
Interface	I/Os	GTs	Rate
8 x 32-bit DDR3	544	-	1600 Mb/s
Interlaken	-	32	10.3 Gb/s

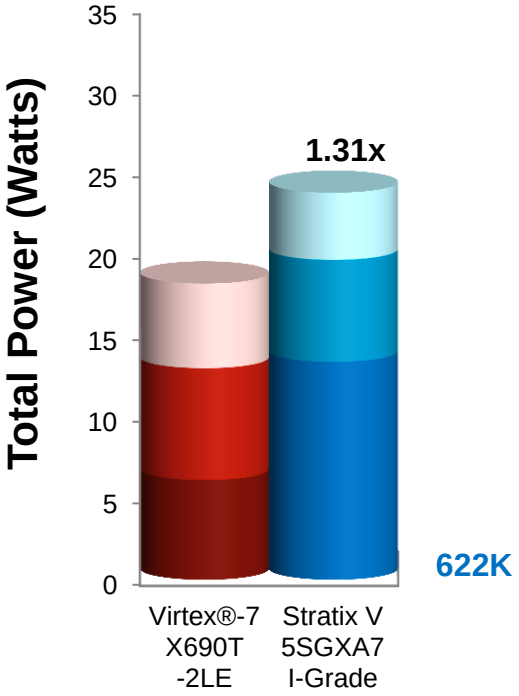
Environment	Process
Tj = 100°C	Max

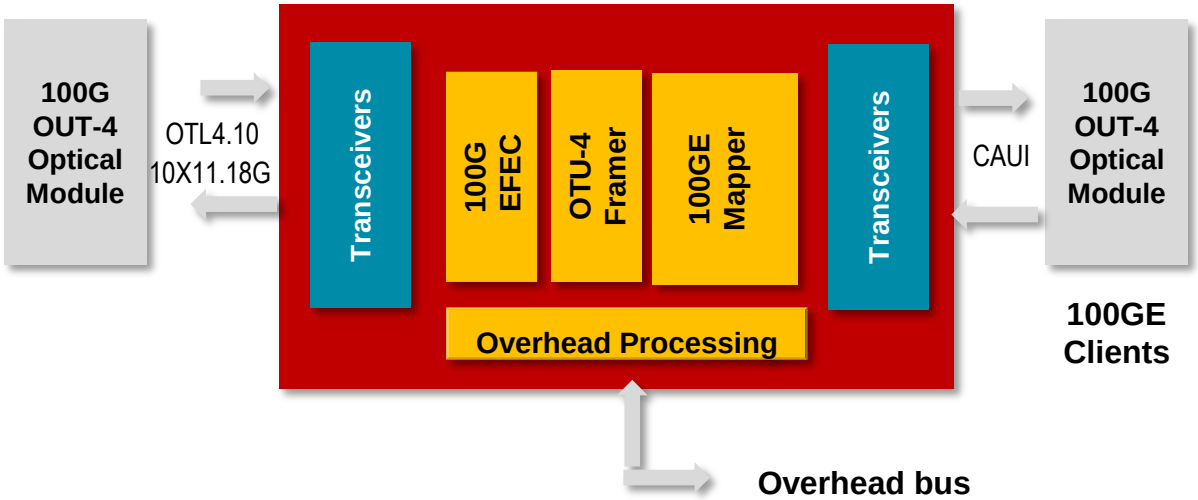
LC/LEs	232K
Flip-Flops	167K
Block RAM	15516 Kb
DSP Blocks	2
PLLs	8
Core Freq.	250 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Power Benchmark: 100GE over OTU4 Transponder Virtex-7 X690T FPGA







Resources

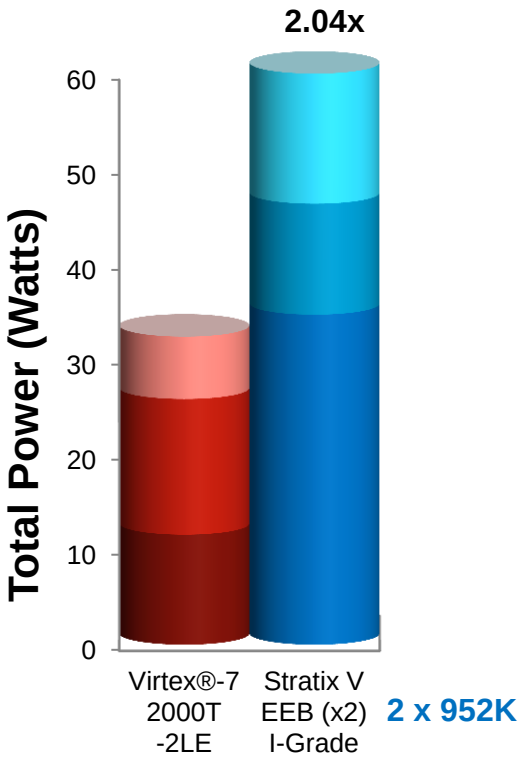
Interface	I/Os	GTs	Rate
LVCMOS	50	-	250 Mb/s
GT	-	10	11.1 Gb/s
GT	-	10	10.3 Gb/s

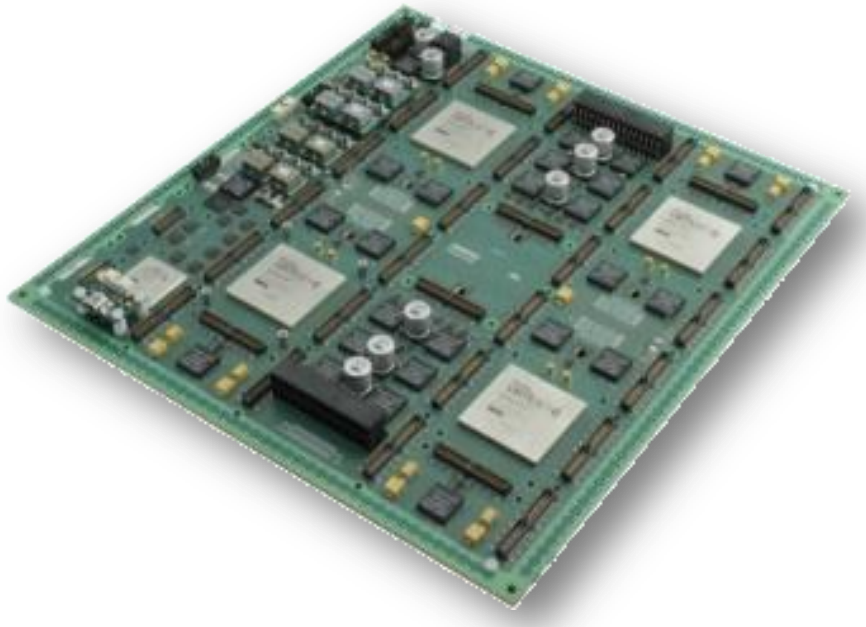
Environment	Process
Tj = 100°C	Max

LC / LEs	392K
Flip-Flops	245K
Block RAM	9,360 Kb
Core Freq.	350, 175 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Power Benchmark: ASIC Prototyping
Virtex-7 FPGA 2000T





Resources

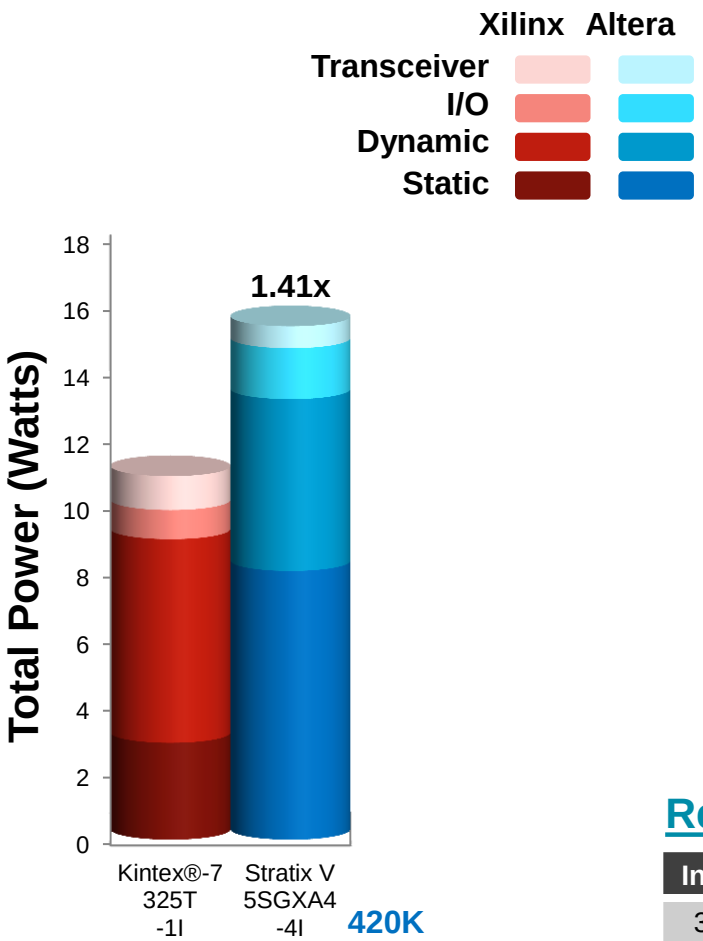
Interface	I/Os	GTs	Rate
3 64-bit DDR3	366	-	1066 Mb/s
LVDS	408	-	1000 Mb/s

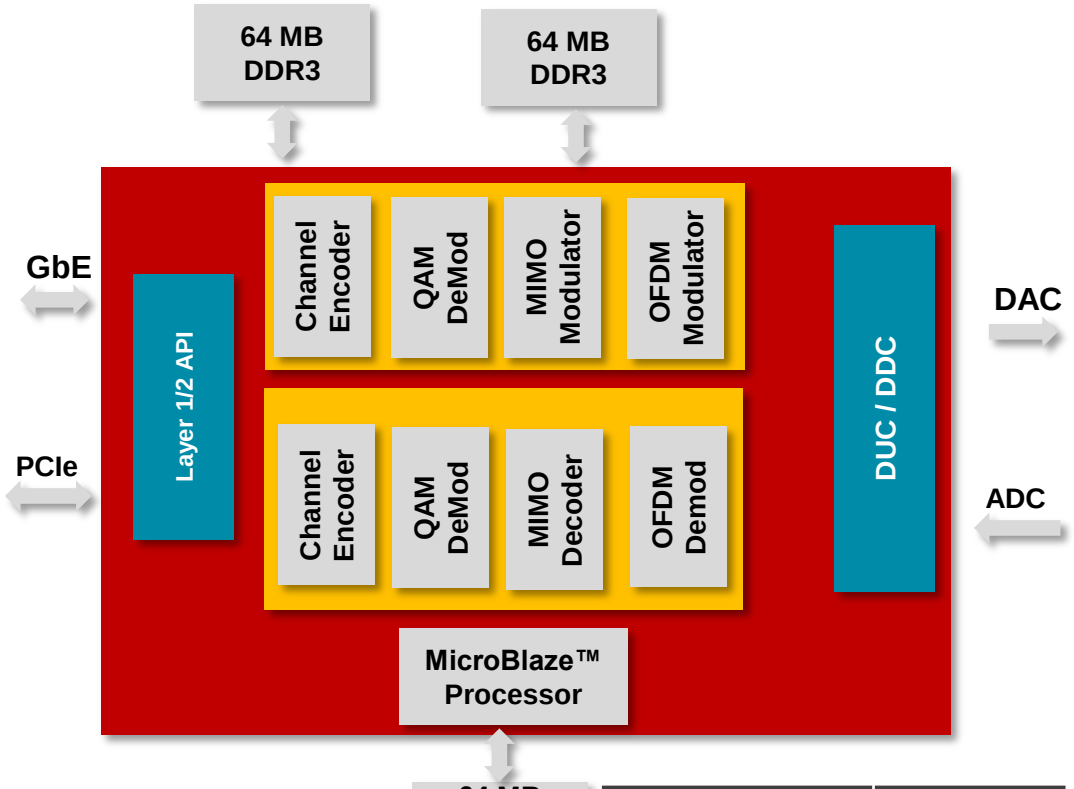
Environment	Process
Tj = 100°C	Max

LC / LEs	1,224K
Flip-Flops	765 K
Block RAM	21,600 Kb
Core Freq.	200 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Power Benchmark: Wireless WCDMA / LTE Picocell Kintex-7 325T FPGA





Resources

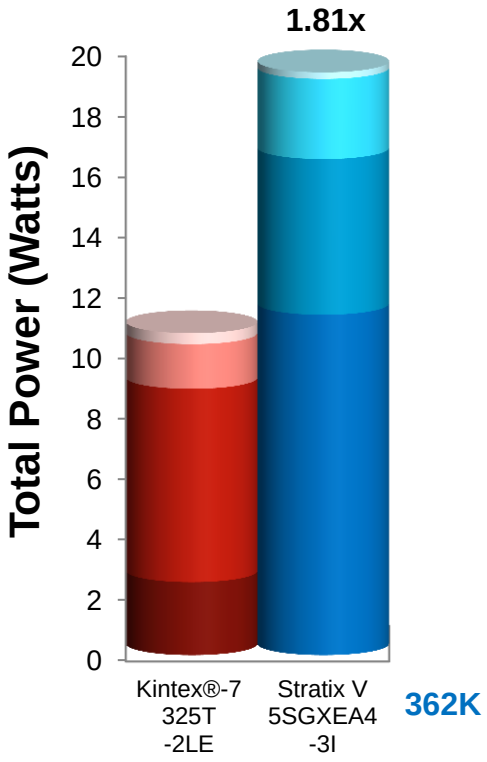
Interface	I/Os	GTs	Rate
3 x 16-bit DDR3	129	-	1066 Mb/s
GT	-	2	4.0 Gb/s
GT	-	1	1.25 Gb/s
GT	-	1	2.5 Gb/s

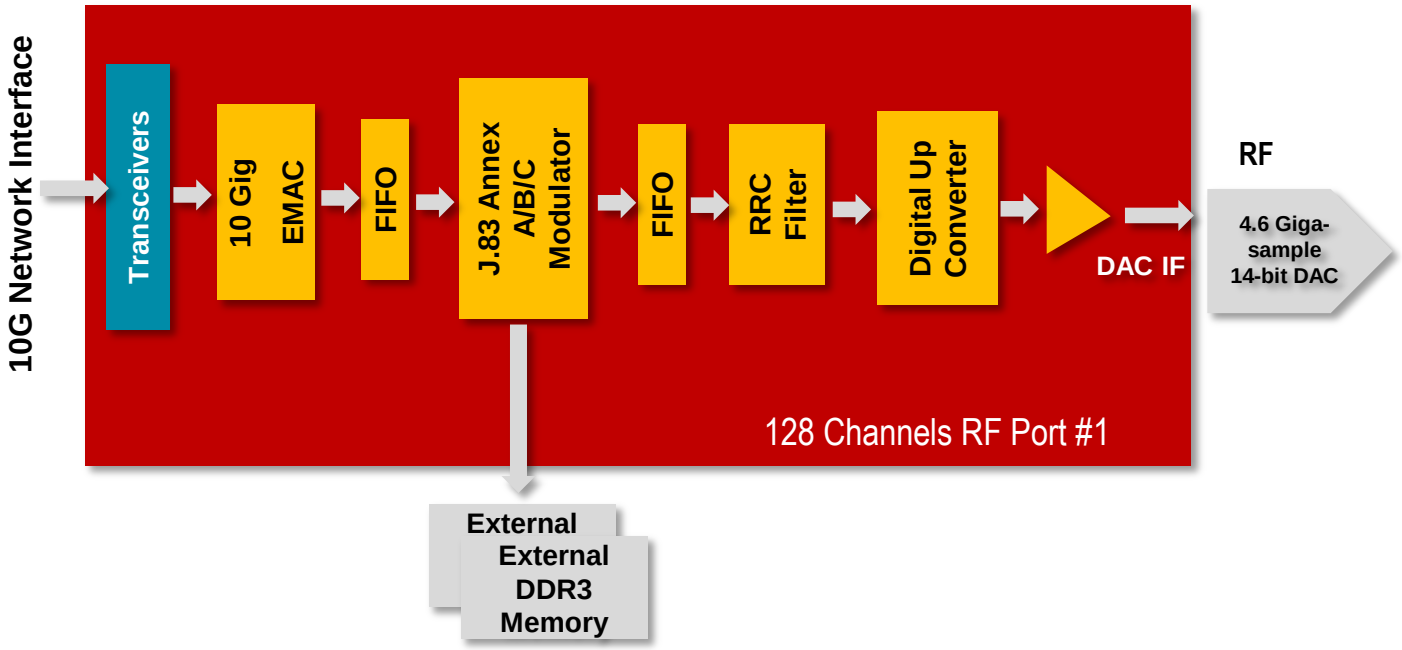
Environment	Process
Tj = 100°C	Max

LC / LEs	240K
Flip-Flops	150K
Block RAM	14,562 Kb
DSP Blocks	342
PCIe® Blocks	1
Core Freq.	307.2 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Dense Edge QAM Modulator
Kintex-7 325T FPGA





Resources

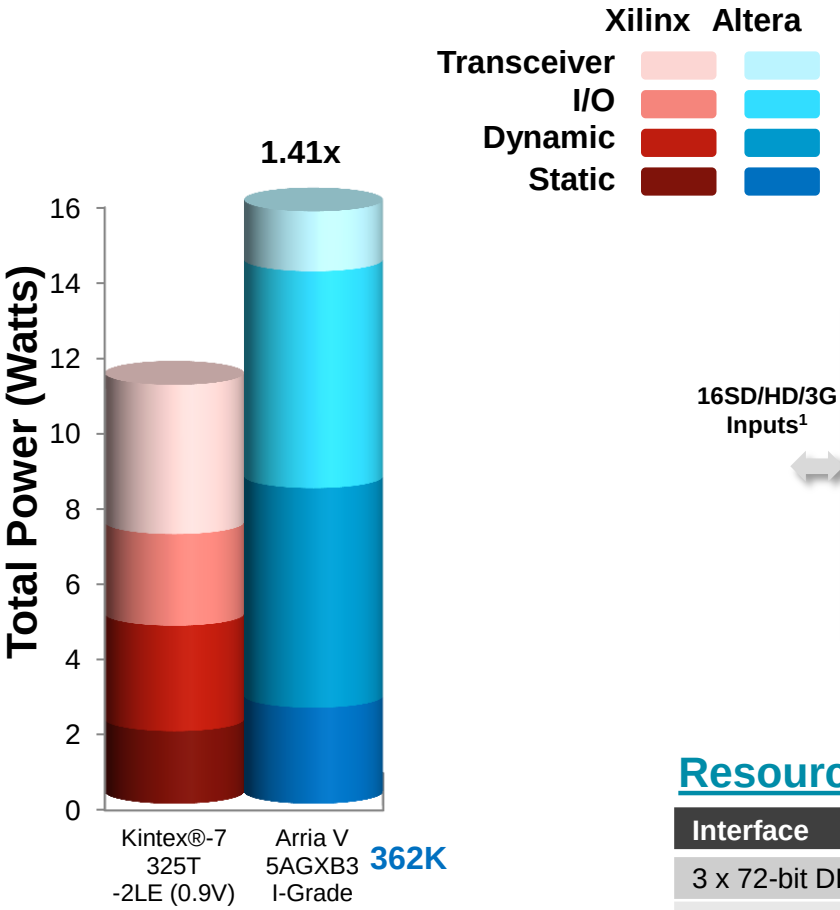
Interface	I/Os	GTs	Rate
LVDS	124	-	1152 Mb/s
LVCMOS	12	-	15 MHz
2x 8-bit DDR3	55	-	800 Mb/s
GT	-	1	10.3 Gb/s

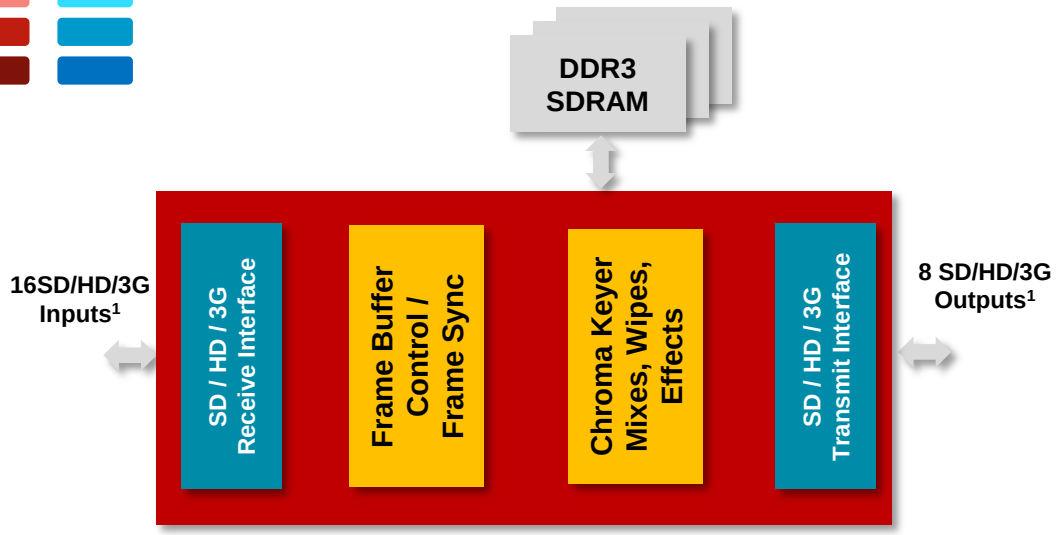
Environment	Process
Tj = 100°C	Max

LC / LEs	182K
Flip-Flops	157K
Block RAM	12,402 Kb
DSP Blocks	641
Core Freq.	384, 576,156, 192, 200 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Power Benchmark: AVB Switcher Kintex-7 325T FPGA





Resources

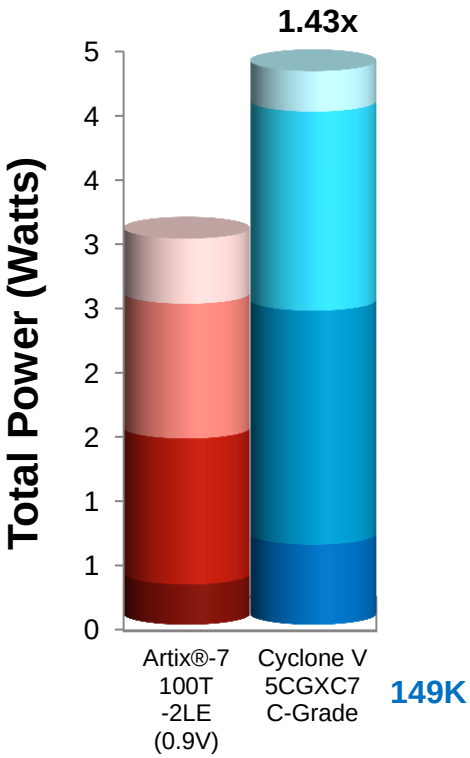
Interface	I/Os	GTs	Rate
3 x 72-bit DDR3	450	-	800 Mb/s
GT	-	16	2.97 Gb/s

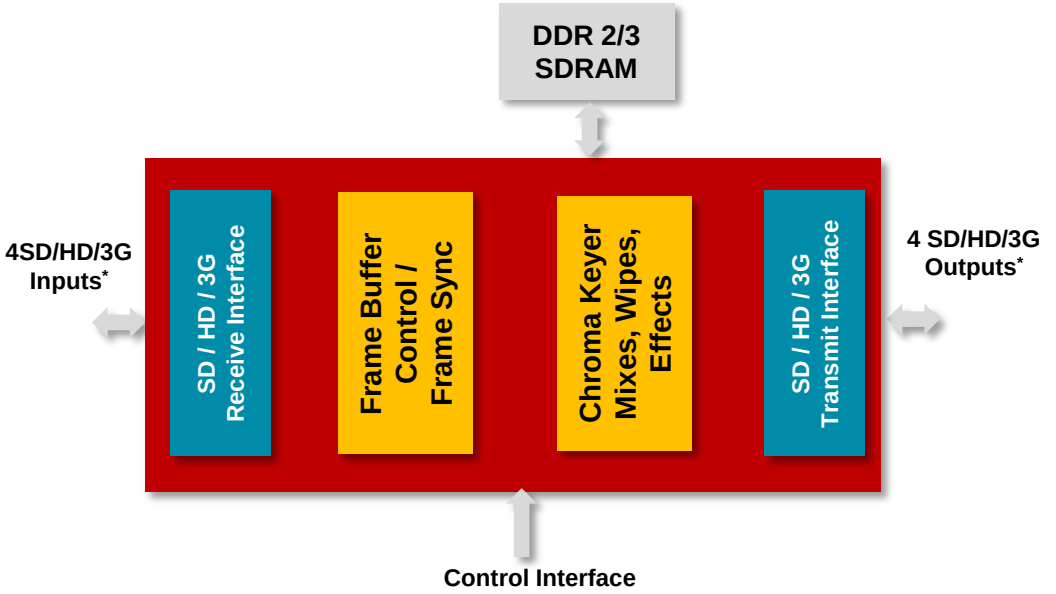
Environment	Process
Tj = 100°C	Max

LC / LEs	300K
Flip-Flops	188K
Block RAM	10,800 Kb
DSP Blocks	500
Core Freq.	148.5 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

AVB Switcher (4-channel)
Artix-7 100T FPGA





*Note: SD/HD/3G inputs and outputs share GTs

Resources

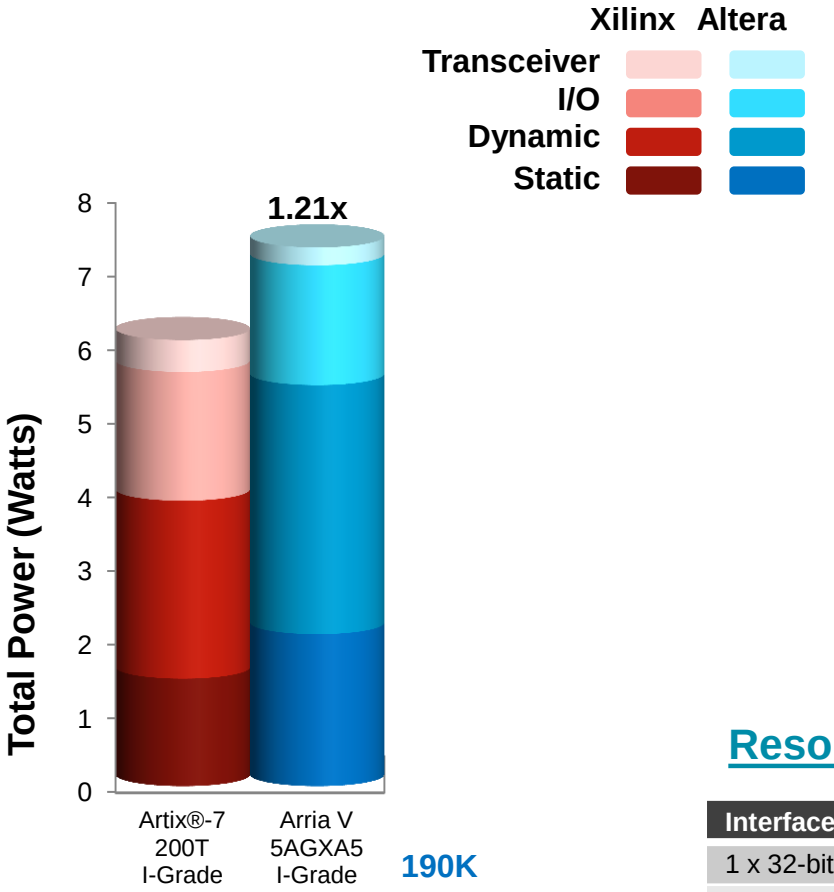
Interface	I/Os	GTs	Rate
1 x 64-bit DDR3	112	-	800 Mb/s
GT	-	4	2.97 Gb/s

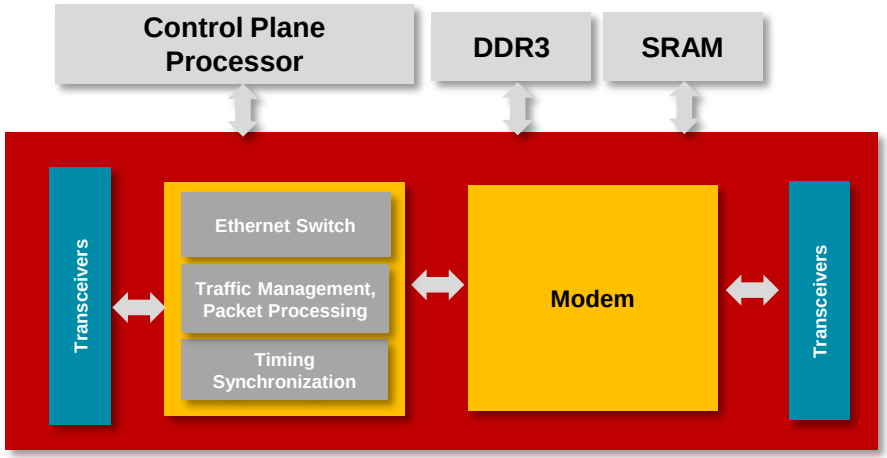
Environment	Process
Tj = 85°C	Max

LC / LEs	75K
Flip-Flops	47K
Block RAM	2,250 Kb
DSP Blocks	125
PLL	1
Phaser Block	1
Core Freq.	148.5, 400 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Power Benchmark: Single Channel Mobile Backhaul Artix-7 200T FPGA





Resources

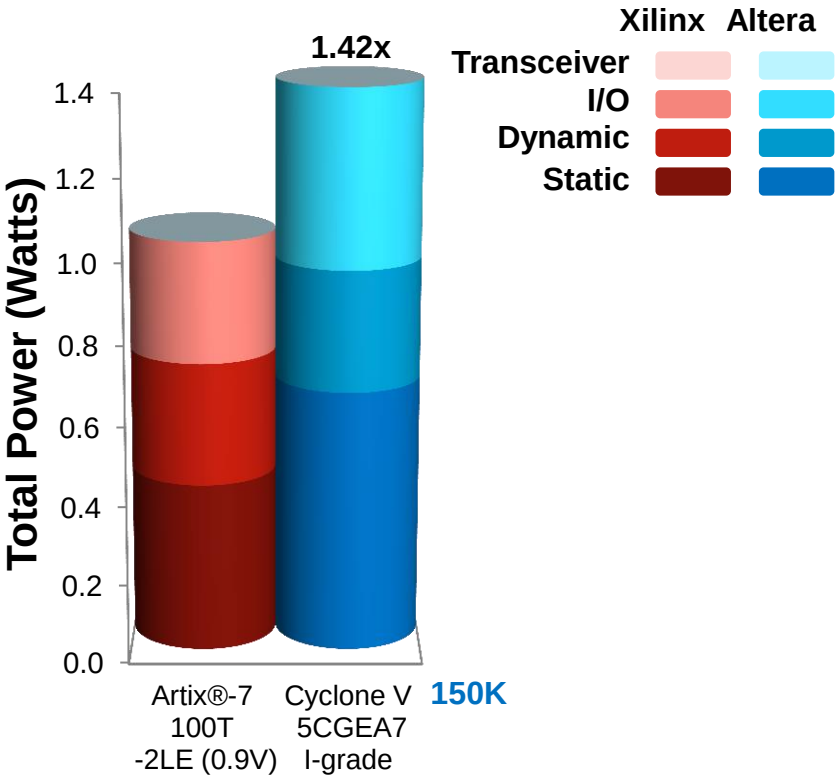
Interfaces	I/Os	GTs	Rate
1 x 32-bit DDR3	72	-	800 Mb/s
LVDS pairs	128	-	800 Mb/s
SEIO	150	-	100 Mb/s
Switch ports	-	4	1.0 Gb/s

Environment	Process
Tj = 100ºC	Max

LC / LEs	130K
Flip Flops	81K
Block RAM	5,076 Kb
DSP Blocks	345
PLL	2
Core Freq.	250, 400 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Power Benchmark: Satellite Modem
Artix-7 100T FPGA



Environment	Process
Tj = 85°C	Max

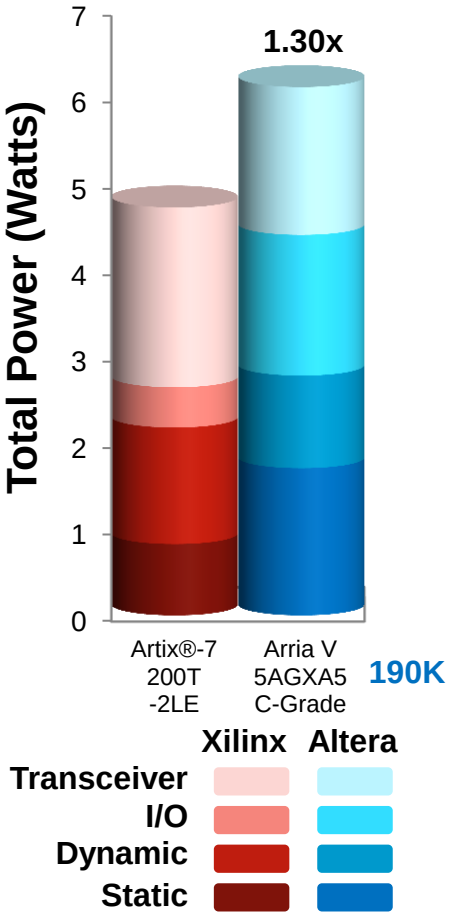
LC/LEs	85 K
Flip-Flops	52 K
Block RAM	3420 Kb
DSP Blocks	126
PLLs	2
Core Freq.	30, 62.5, 125 MHz

Resources

Interface	I/Os	GTs	Rate
1x 32-bit DDR2	69	-	250 Mb/s

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0

Military Network Protocol Platform Data Aggregator Artix-7 200T FPGA



Resources

Interface	I/Os	GTs	Rate
2x 36-bit RLDRAMs	122	-	520 Mb/s
GT	-	6	5 Gb/s
GT	-	8	2.5 Gb/s
GT	-	1	2.5 Gb/s

Environment	Process
Tj = 85°C	Max

LC / LEs	63K
Flip Flops	58K
Block RAM	3600 Kb
DSP Blocks	400
PCIe® Blocks	1
Core Freq.	125 MHz

*Design results sourced from Xilinx Power Estimator (XPE) version 2014.2 and Altera Early Power Estimator (EPE) version 14.0