CoolRunner™-II

Xilinx CoolRunner-II: RealDigital CPLDs

High performance and ultra-low power consumption with no compromises.

The CoolRunner™-II CPLD family utilizes our second-generation RealDigital technology to give you high performance, advanced features, and low power consumption, all at a very low price. Featuring a 100% digital core, up to 323 MHz performance, and low stand-by current, CoolRunner-II CPLDs offer a wide range of densities, plus abundant I/O, the flexibility to move from one density to another in the same package, and the lowest cost per I/O pin in the industry.

Xilinx RealDigital CPLDs eliminate the high-current sense amplifier technology traditionally used in CPLD products. The result is a scalable technology that is ideal for many high volume applications, such as PDAs, cell phones, routers, and high-speed Internet modems.

A Complete Programmable Solution

- **Up to 323 MHz performance** — High performance for leading-edge applications. Up to 500 MHz toggle rate with clock doubler.
- **Ultra-Low standby current** — The industry's lowest power consumption.
- **1.8 Volt device operation** — I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels to simplify multi-voltage system design.
- **A wide range of densities** — From 32 to 512 macrocells, to suit a broad range of applications.
- **Advanced system features** — Multiple I/O standards, clock management, and increased design security simplify your design.
- **Complete software support** — All Xilinx ISE software packages provide complete support for CoolRunner-II devices.
- **Advanced packaging** — Choose from Chip Scale (CSP), QFG, TQFP, PQFP, VQFP, PLCC, and fine line BGA packages for PC board space savings, cost optimization, and high performance. The world's smallest CPLD package, the 5 by 5 mm QFG32, is also available. All packages available in a Pb-Free option.
- **Easy In-System Programming (ISP)** — Support for IEEE 1532 In-System Programming and IEEE 1149.1 JTAG Boundary Scan testing.
- **Superior pin-locking** — Implement design updates without changing pinouts, minimize PC board layout changes and enable field upgradeability.

XILINX®

Advanced System Features

Advanced I/O Support

- **LVTTL and LVCMOS** for standard chip-to-chip interfacing.
- **SSTL and HSTL** for standard chip-to-memory interfacing.
- **DataGATE** disables unused pins to reduce power.
- **Bus Hold** keeps outputs in their last stable state, for further power reduction.
- **Input hysteresis (500mv)** conditions noisy and slow transitioning signals.

Superior Clock Management

- **DualEDGE Registers:** Enhances performance by doubling input clock switching frequency.
- **Clock Divider:** Improves power savings by dividing externally supplied global clocks by standard values.
- **CoolCLOCK:** Combines a clock divider and doubler to divide an incoming clock by two (reducing clocking power), and then doubling the clock at the macrocell.

Unparalleled Design Security

- **Four levels of design security** prevent accidental overwriting and pattern theft.

Free Reference Designs

- MP3 Player
- UARTs and bus controllers
- PicoBlaze microcontroller
- And many more

Software Tools

CoolRunner-II CPLDs are supported in all versions of the Xilinx Integrated Software Environment (ISE) which include ISE WebPACK™, and ISE Foundation™.

- **ISE WebPACK** is a free, downloadable desktop solution that offers HDL and ABEL synthesis and simulation, schematic entry, JTAG and third-party EDA support, and device support for all CPLD families (as well as Virtex™-4, Virtex-II Pro, Virtex-II, Virtex-E, Spartan™-3E, Spartan-3, Spartan-IIE, and Spartan-II)
- **ISE Foundation** is the full featured software environment that supports all of our current CPLD and FPGA families.

DOWNLOAD NOW

For additional information, please visit our website at:
www.xilinx.com/cr2

CoolRunner-II Family at a Glance

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
I/O Standards	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1
Max I/O	33	64	100	184	240	270
T_{PD}(ns)	3.8	4.6	5.7	5.7	7.1	7.1
I/O Banks	2	2	2	2	4	4
DualEDGE Registers	Yes	Yes	Yes	Yes	Yes	Yes
Input Hysteresis	Yes	Yes	Yes	Yes	Yes	Yes
DataGATE & Clock divide	—	—	Yes	Yes	Yes	Yes
Packages	QFG32 VQ44 PC44 CP56	 VQ44 PC44 QFG48 CP56 VQ100	 VQ100 CP132 TQ144	 VQ100 CP132 TQ144 PQ208 FT256	 TQ144 PQ208 FT256 FG324	 PQ208 FT256 FG324

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Tel: (408) 559-7778
Fax: (408) 559-7114
Web: www.xilinx.com

European Headquarters
Xilinx
Citywest Business Campus
Saggart,
Co. Dublin
Ireland
Tel: +353-1-464-0311
Fax: +353-1-464-0324
Web: www.xilinx.com

Japan
Xilinx, K.K.
Shinjuku Square Tower 18F
6-22-1 Nishi-Shinjuku
Shinjuku-ku, Tokyo
163-1118, Japan
Tel: 81-3-5321-7711
Fax: 81-3-5321-7765
Web: www.xilinx.co.jp

Asia Pacific
Xilinx Asia Pacific Pte. Ltd.
No. 3 Changi Business Park Vista, #04-01
Singapore 486051
Tel: (65) 6544-8999
Fax: (65) 6789-8886
RCB no: 20-0312557-M
Web: www.xilinx.com

Distributed By:

FORTUNE 2005 100 BEST COMPANIES TO WORK FOR

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Printed in the U.S.A.

PN 0010619-02