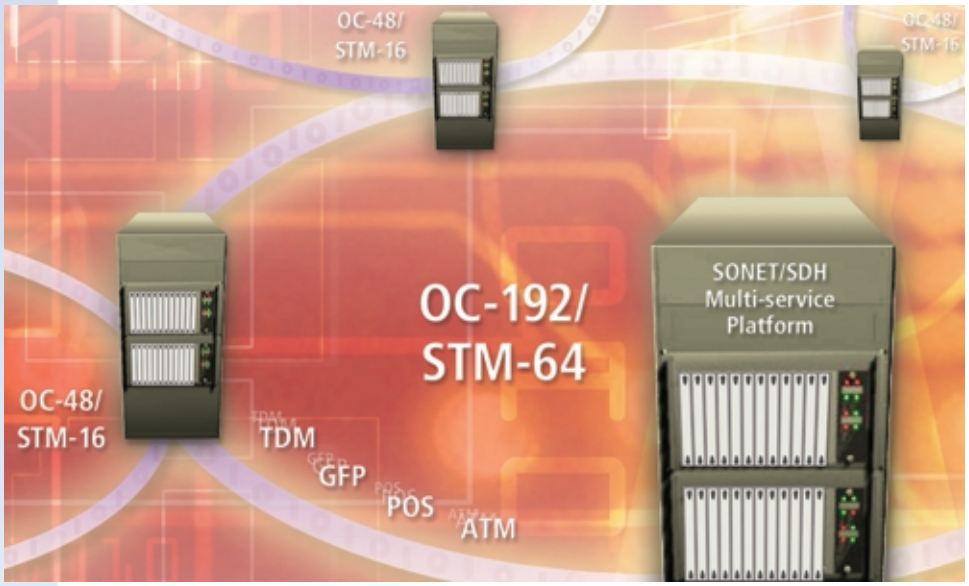
Xilinx® Solutions for SONET/SDH Equipment

Data traffic over SONET/SDH networks has increased dramatically with the proliferation of the Internet and enterprise networks. As a result, equipment traditionally supporting only voice traffic such as add/drop multiplexers and digital cross connects must now also support multiple data protocols, faster data rates, and denser port counts. Next-generation SONET/SDH systems are "multi-service" and more powerful, but also face a host of design challenges, especially in the area of flexibility.

To meet these challenges, Xilinx offers end-to-end SONET/SDH solutions that support designs with 10G SONET/SDH, SerDes, OIF 10G standards, and IP for OC-192/STM-64 framing.

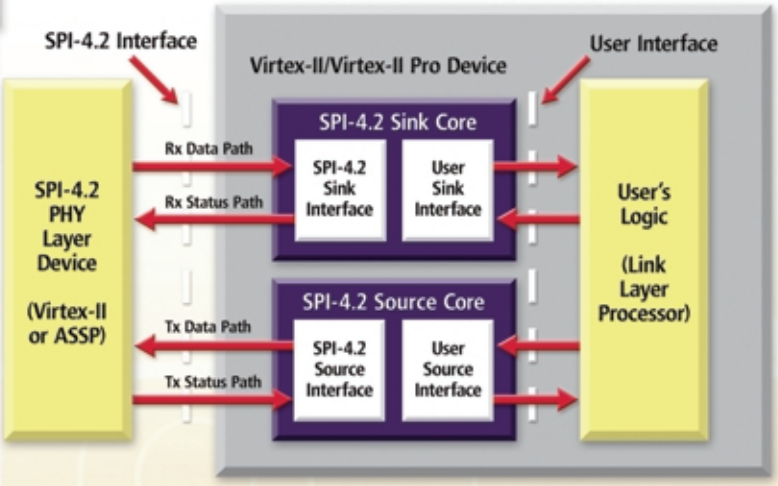
Xilinx and our Global Alliance partners also provide a variety of IP for data over SONET, SONET/SDH-system interfaces and memory controllers, as well as several soft- and hard-core embedded processor options. From line-side to backplane, Xilinx is the best choice for your SONET/SDH needs.



End-to-end SONET/SDH Connectivity and Functionality

Benefits of using Xilinx include:

- **10G Optical Module Capabilities –** Implement mux/demux in 300-pin MSA transponders and drive XFP transceivers with the lowest-cost single-chip 10G RocketPHY™ SerDes.
- **2.5G SFP Module –** Module capabilities with Virtex-II Pro X
- **SPI-4.2 and SFI-4.1 Connectivity –** Implement 10G OIF interface standards with Xilinx's industry-leading SPI-4.2 IP core and I/Os supporting 622Mbps SDR LVDS for SFI-4.1 interfaces.
- **Large Library of SONET/SDH Soft IP –** Implement SONET/SDH protocol processing functions such as OC-n/STM-n, T1/E1 and T3/E3 framing, Digital Wrapper, error correction for 10 Gpbs OC-192 and 40 Gbps OC-768 systems, and Ethernet/ATM/IP mapping over SONET/SDH. Also available are interface IP solutions such as SPI-3, Utopia L2, and more.
- **Processor Core Offerings –** Choose from the 32-bit IBM PowerPC™ 405 hard core immersed in Virtex-II Pro or the 32-bit MicroBlaze RISC soft processor core. Or use the PicoBlaze 8-bit micocontroller reference design in your SONET/SDH system.
- **Free Memory Controller Reference Designs –** Save time by using Xilinx memory controller reference designs such as RLDRAM, FCRAM, QDR SRAM, SDRAM, SDRAM/DDR, available free at the Xilinx website.
- **Ultimate Backplane Connectivity –** Embedded RocketIO™ and RocketIO X SerDes for 622 Mbps up to 10.709 Gbps, flexible SelectIO™-Ultra I/O blocks, and a large library of IP for standard interfaces make Xilinx ideal for back-plane connectivity. Enable architectures including LVDS-based parallel back-planes, full-mesh serial backplanes based on Gigabit Ethernet, XAUI, PCI Express™, Aurora, SONET/SDH, and more.



OIF Connectivity with SPI-4.2 and SFI-4.1 Solutions

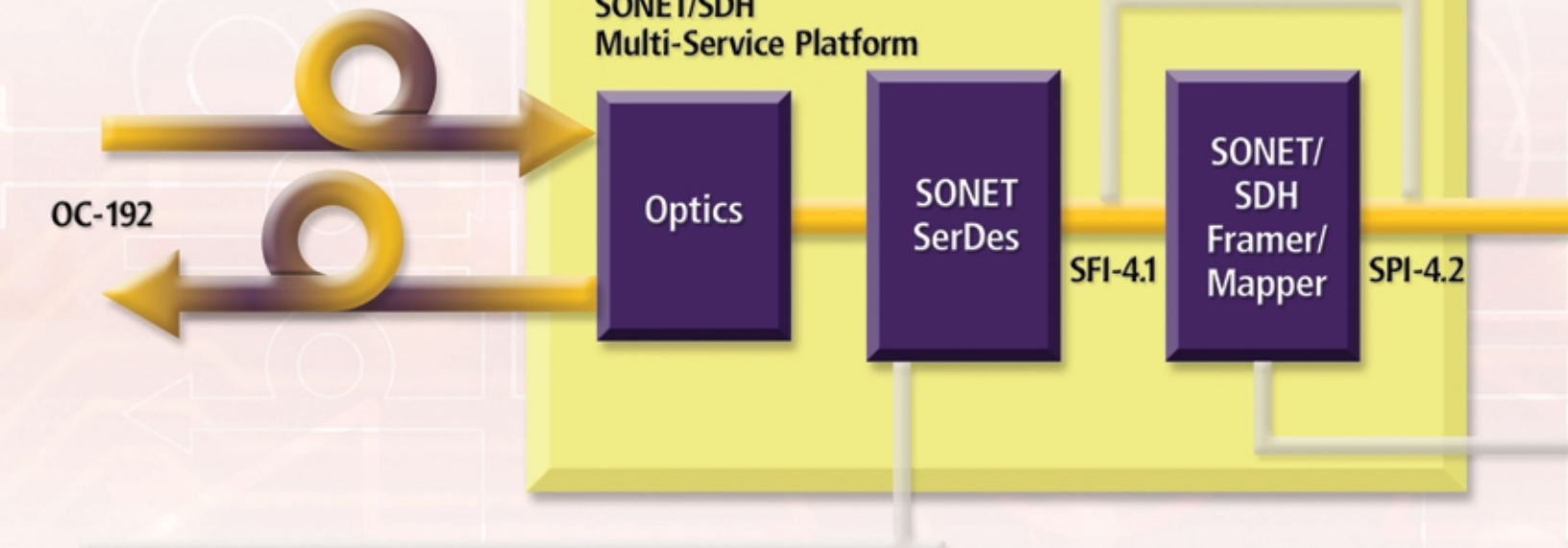
Industry Leading SPI-4.2 Soft IP Core

- Fully compliant to OIF SPI-4.2 specification
- 1 to 256 channels; 64, 128-bit user interface
- Source bandwidth efficiency – no idle cycles inserted; combined EOP/SOP
- Dynamic phase alignment allows per-bit deskew
- Low power, efficient utilization
- Sink core support for contiguous EOP bursts
- "Lite" version available – cost optimized for 2.5G

622 Mbps LVDS I/Os for SFI-4.1

- Xilinx I/Os supports up to 644 Mbps SDR LVDS operation to enable SFI-4.1 (622 Mbps) and XSBI (644 Mbps) interfaces. This is detailed in the reference design "XAPP622: 644-MHz SDR LVDS transmitter/receiver."

LogiCORE Reference DESIGN



SONET/SDH SerDes Solutions

Discrete 10G RocketPHY SerDes

- Exceeds OC-192/STM-64 jitter generation, jitter transfer, jitter tolerance specifications
- 9.9532 Gbps SONET data rate; also supports SONET w/FEC and 10Gb Ethernet
- CDR, CMU, 16-bit data path
- Applications: 300-pin MSA, XFP MSA
- Supports SFI-4.1; 16-bit LVDS I/F (DDR/SDR)

SONET/SDH Soft IP

Softcore SONET/SDH IP is available from Xilinx LogiCORE and AllianceCORE partner libraries.

SONET/SDH

- OC-192/STS-192/STM-64 framer & path processor
- OC48 framer & path processor
- OC-3/-12 framer

G.709 Framing (w/ or w/out FEC)

- G.709 STS-192 framers
- G.709 STS-48 framers
- G.709 standalone FEC (G.975)

Error Correction

- CRC-32 for 10 Gbps OC-192 systems
- CRC-32 for 40 Gbps OC-768 systems

LogiCORE

XILINX®

Processing Core Offerings

Xilinx provides several options for your microprocessing needs in SONET/SDH systems

IBM PowerPC 405 Hard Core
- Hard IP, embedded in Virtex-II Pro
- 32-bit/400 MHz/600 + DMIPs
- Up to 4 per device

Soft Processor
- MicroBlaze – 32-bit RISC/150 DMIPs/125 MHz
- PicoBlaze 8-bit microcontroller reference design/40-70 MIPS

Applications
- Control-plane processing, configuration management, statistics gathering, general-purpose I/O

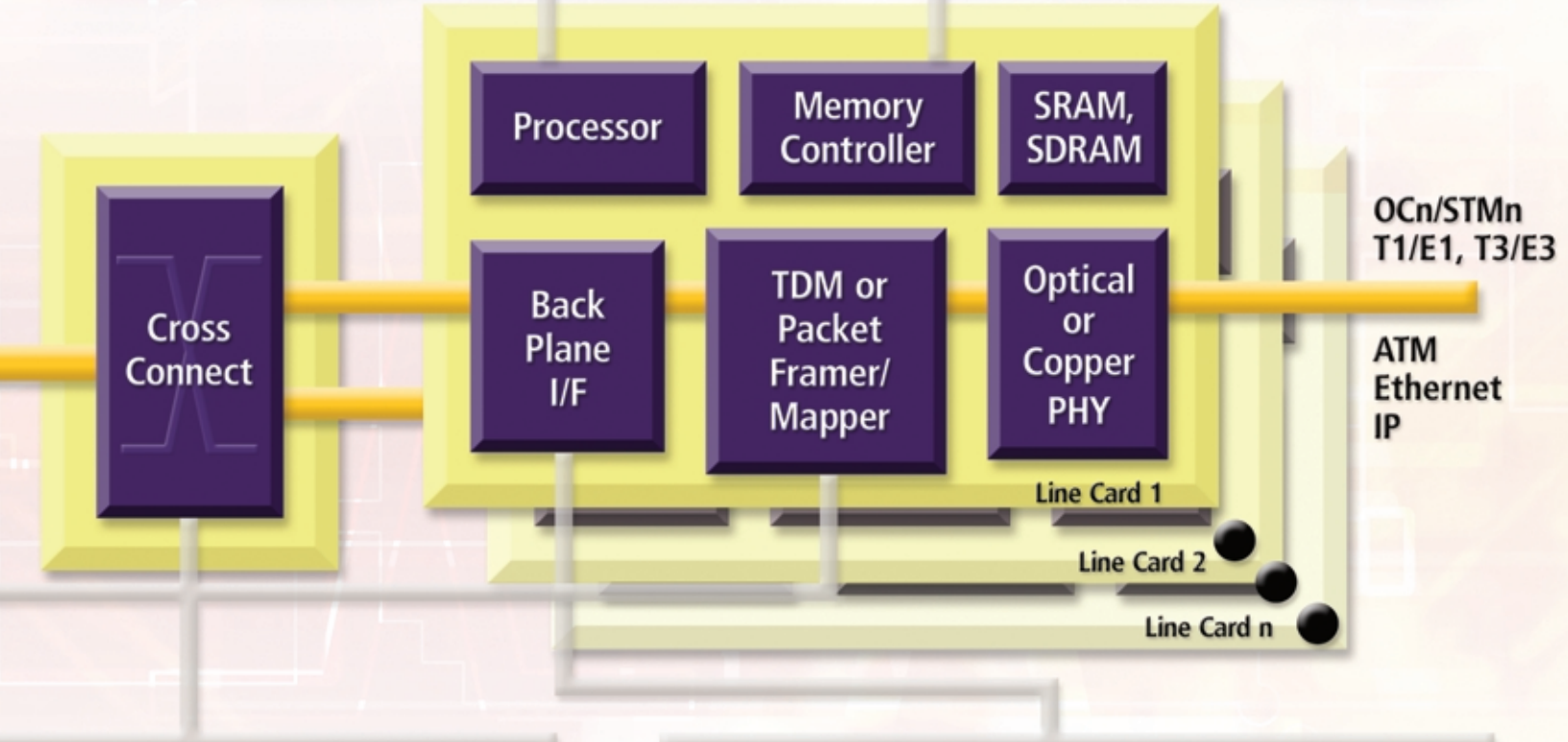
PowerPC™ MicroBlaze™ PicoBlaze™

Memory Controller Solutions

IP cores from partners and free reference designs from Xilinx, covering various memory controllers can be found on the Xilinx website.

- DDR/SDR SDRAM
- FCRAM
- CAM
- QDR SRAM
- RLDRAM
- Sigma RAM
- ZBT/NoBL SRAM
- SDRAM

Alliance CORE™ Reference DESIGN



Data over SONET
- 10Gbps, 1Gbps, 10/100 Mbps Ethernet MACs
- GFP framers (10G and 2.5G)
- ATM cell processor
- HDLC (single & multi-channel)
- PPP8

PDH
- T1/E1 and T3/E3 framers

System Interfaces
- SPI-4.1, SPI-3, telecom bus
- SPI-4.1 to XGMII, SPI-4.2 to SPI-3

Cross-Bar Switch

Alliance CORE™

Backplane Solutions

Embedded RocketIO and RocketIO X SerDes, Virtex-II Pro and Virtex-II Pro X FPGAs
- Full-duplex SerDes; 622 Mbps to 10.709 Gbps
- Tx pre-emphasis, variable output voltage, channel bonding, CDR, clock synthesis

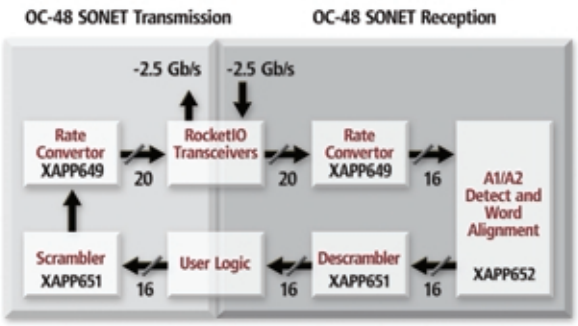
RocketIO™ RocketIO X™

SelectIO-Ultra Parallel I/O
- Up to 1200 user I/Os supporting over 25 single-ended and differential standards (840 Mbps LVDS)

System Interfaces Supported
- XAUI, XGMII, GMII, SPI-4.2, (with dynamic phase alignment) Aurora, PCI Express, RapidIO™, HyperTransport™, InfiniBand™, Fibre Channel, CSIX, PCI/PCI-X, and more

SONET Backplane Application Notes

Learn how to create highly integrated and flexible OC-48/OC-192 transmit/receive elements over backplanes using Virtex-II Pro FPGAs with the following reference designs.



- Rate Conversion in Virtex-II Pro Devices (XAPP649)*
- Transmission Scrambler/Descrambler (XAPP651)
- Word Alignment and Deframing (XAPP652)

* No rate conversion is necessary in Virtex-II Pro X which has built-in x8, x16 datapath and x16 clocking.

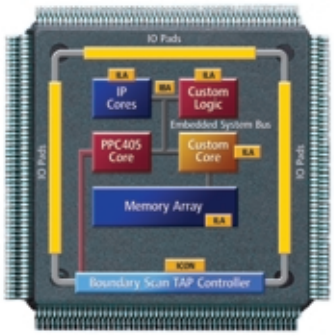
Xilinx and Partner IP and Reference Designs

For a complete listing of all of Xilinx available application notes, reference designs and IP cores, please visit **http://www.xilinx.com/ipcenter.**

ChipScope Pro

Designers of FPGA-based SONET/SDH systems can use the ChipscopePro suite of tools to quickly and easily debug large, sophisticated designs.

- Embed Logic Analyzer (ILA) and Bus Analyzer (IBA) cores to view all internal FPGA signals and nodes
- Supports IBM CoreConnect Processor Local Bus (PLB) or On-Chip Peripheral Bus (OPB) for the PowerPC 405



Partner Reference Designs

Xilinx has collaborated with several partners to provide reference designs for SONET/SDH applications, including:

- WestBay/Intel WB4500 OC48/12 multiprotocol VC framer
- Cypress "Fiber-to-Fiber" data over SONET/SDH solution
- Ignis Optics 2.5 Gbps SFP module
- AMCC nPC1515 SPI4-to-VIX3 bridge
- Bay MicroSystems Montego NPU
- Velio and BitBlitz telecom/datacom SerDes
- NetLogic and SiberCore CAM
- Zettacom and Teracross traffic managers

All available reference designs are detailed at **http://www.xilinx.com/company/reference_design/**

Xilinx and XPERTs Partners Design Services

Customers can leverage Xilinx Design Services (XDS) and XPERTs partners' experience and expertise in SONET/SDH systems for design consultation, complete custom IP and design creation, and project management. Areas of experience include:

- **Networking & Telecom –** SONET/SDH (framing, overhead processing, data path controllers), ATM (adaptation layer processing, switching, termination, Utopia), Ethernet (MAC processing, PPP termination), TDM, HDLC, FEC
- **System Interfaces –** SPI-4, SPI-3 UTOPIA master/slave, and more

Visit **http://www.xilinx.com/xds** to see what XDS offers.
Visit **http://www.xilinx.com/company/consultants/index.htm** to see what our XPERTs partners have to offer.

Visit our eSP Portal for Metro Access Networks

The Xilinx eSP Metro Access Networks portal includes technology tutorials, case studies/use models, IP solutions, system block diagrams, reference designs, industry links, white papers, and more. Visit this valuable resource today at: **http://www.xilinx.com/esp/optical/net_tech/sonet.htm**

eSP WEB PORTAL

VIRTEX-II PRO X VIRTEX-II PRO VIRTEX-II RocketPHY

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