



DOMAIN-SPECIFIC METHODOLOGY  
FOR XILINX TARGETED DESIGN PLATFORMS

### » Steep Digital Design Challenges

- Reducing design iterations to meet aggressive deadlines
- Achieving greater performance, lower cost, and reduced power
- Addressing growing design complexity and domain-specific requirements
- Addressing the demands for product differentiation

### » The ISE Design Suite

- Achieve greater designer productivity
- Focus on design differentiation
- Shrink time to production
- Attain breakthrough performance, power, and cost benefits

### Unlock New Levels of Productivity

The ISE® Design Suite 12 software unlocks greater design productivity with breakthrough technologies for power optimization and cost. The Design Suite enables the fastest time to design completion with Xilinx Targeted Design Platforms — available in four different configurations aligned to user preferred methodology—logic, embedded, DSP, or system design.

Available starting with the ISE Design Suite 12 release:

- “Intelligent” clock-gating technology that reduces dynamic power consumption by as much as 30 percent
- Advances in timing-driven design preservation, AMBA® 4 AXI™-4-compliant IP support for plug-and-play design
- Intuitive design flow with fourth-generation partial reconfiguration capabilities that lowers system cost for a broad range of high performance applications

### Complete Methodology for Targeted Design Platforms

Xilinx Targeted Design Platforms provide embedded, DSP, and hardware designers alike with access to a wide array of silicon devices supported by open standards, common design flows, IP, and run-time platforms. The ISE Design Suite brings it all together with domain-specific design environments, while enabling design teams to meet their power and performance goals with Xilinx CPLDs and FPGAs, including the new Virtex®-6 and Spartan®-6 families.

### Integrating System-Level Design

ISE Design Suite provides a tight connection between embedded and DSP flows to enable integration of designs that contain embedded, DSP, IP, and user blocks in one system. To better serve users familiar with differing design environments, the ISE Design Suite 12 provides specific accommodations for designers ranging from the pushbutton user to the ASIC designer.

Visit [www.xilinx.com/ise](http://www.xilinx.com/ise) to download a free 30-day evaluation, or to learn more about the Xilinx Targeted Design Platforms.

## ISE Design Suite: Logic Edition

The ISE Design Suite: Logic Edition delivers a complete solution for logic and connectivity design, providing the front-to-back base methodology and IP. The Logic Edition includes:

- New Design Preservation flow to improve timing predictably
- Partial Reconfiguration supporting Virtex-6 FPGA in ISE Design Suite 12.2
- Intelligent Clock-Gating supporting Virtex-6 in ISE Design suite 12.1 and Spartan-6 in ISE Design Suite 12.2
- Plug-and-play FPGA design through AMBA® 4 AXI™-4 interconnect protocol IP in ISE Design Suite 12.3

These new capabilities are in addition to the Xilinx-exclusive tools and technologies for design entry, synthesis, implementation, and verification to help achieve optimal design results in the shortest time.

For more information visit [www.xilinx.com/ise-logic](http://www.xilinx.com/ise-logic).

## ISE Design Suite: Embedded Edition

The ISE Design Suite: Embedded Edition delivers all of the features, technologies, and IP found in the Logic Edition plus additional tools, including the IP, required for FPGA designs with embedded PowerPC® hard processor and/or MicroBlaze™ soft processor cores. Designers have access to the Xilinx Platform Studio (XPS) tool suite, which delivers a graphical environment and command line support for developing hardware platforms for embedded applications. The ISE Design Suite: Embedded Edition 12.3 will support plug-and-play FPGA design and IP-optimized for embedded using AMBA AXI4 interconnect protocol IP.

For more information visit [www.xilinx.com/ise-embedded](http://www.xilinx.com/ise-embedded).

## ISE Design Suite: DSP Edition

The ISE Design Suite: DSP Edition addresses the unique needs of the DSP design methodology. In addition to the tools, technologies, and IP in the Logic Edition, the DSP Edition includes System Generator for DSP and specialized IP required for DSP development. With System Generator for DSP, developers with little FPGA design experience can quickly create production-quality FPGA implementations of DSP algorithms in a fraction of traditional RTL development times. The ISE Design Suite: DSP Edition 12.3 will support plug-and-play FPGA design and IP-optimized for embedded using AMBA AXI4 interconnect protocol IP.

For more information visit [www.xilinx.com/ise-dsp](http://www.xilinx.com/ise-dsp).

## ISE Design Suite: System Edition

The ISE Design Suite: System Edition includes all of the tools, technologies, and IP from the Logic, DSP, and Embedded Editions. The System Edition delivers a flexible solution for the user who requires a unique methodology that allows powerful DSP functionality in an embedded design or who wants to dramatically extend DSP designs through embedded processor capabilities.

For more information visit [www.xilinx.com/ise-system](http://www.xilinx.com/ise-system).

## FEATURE COMPARISON TABLE

FEATURES	ISE WEBPACK™ (DEVICE LIMITED)	LOGIC EDITION	EMBEDDED EDITION	DSP EDITION	SYSTEM EDITION
ISE Foundation with ISE Simulator (ISim)	●	●	●	●	●
PlanAhead™ Design and Analysis Tool	●	●	●	●	●
ChipScope™ Pro and the ChipScope Pro Serial I/O Toolkit		●	●	●	●
Embedded Development Kit* (EDK)			●		●
Software Development Kit* (SDK)			●		●
System Generator with DSP				●	●

\*Available as a standalone product

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