The Ultimate System Integration Platform

VIRTEX-5 FPGAs

Built-in PCIe & Ethernet Blocks
PowerPC 440
580 GMACS DSP
65nm ExpressFabric Technology
The Virtex®-5 family of FPGAs offers a choice of four new platforms, each delivering an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing:

- Optimized for high-performance logic
- Optimized for high-performance logic with low-power serial connectivity
- Optimized for DSP and memory-intensive applications, with low-power serial connectivity
- Optimized for embedded processing and memory-intensive applications, with highest-speed serial connectivity

All platforms are backed by complete solutions including design tools, IP, development boards, protocol-specific characterization reports, training, services, support, and more.

Discover how this new family delivers even higher performance, lower power, and lower system cost than previous-generation, Virtex-4 FPGAs.

Meet Your Performance Targets Easily

- Achieve a two speed-grade performance gain with new ExpressFabric™ technology
- 550 MHz clocking technology and performance-tuned IP blocks
- 1.25 Gbps LVDS I/O: up to 600 pin pairs (1,200 I/Os)
- 580 GMACS performance from DSP48E slices
- 1,100 DMIPS per PowerPC® 440 processor block with high-bandwidth, low-latency interfaces

Optimize I/O Bandwidth, Power and Cost with Easy-to-Use High-Speed Serial Solutions

- RocketIO® GTP transceivers in the LXT and SXT platforms deliver lowest-power serial connectivity: less than 100 mW (typ) per transceiver at 3.75 Gbps
- RocketIO GTX transceivers in the FXT platform deliver highest-performance serial connectivity: 150 Mbps – 6.5 Gbps
- First FPGA family with hardened PCI Express® endpoint blocks and Tri-mode Ethernet MACs

Beat Your Power Budget while Maximizing Performance

- 35% lower dynamic power with 65nm ExpressFabric technology and power-saving IP blocks including PCI Express endpoint, Gigabit Ethernet MAC, and PowerPC 440 processor
- Further reduce dynamic power consumption by an average 10% with interactive power analysis tools
- Simplify design with no need to select different power supply voltages for high performance versus low power
- Reduce system complexity and cost through fewer power supply rails, fewer regulators, and reduced board area

Build Highest-Performance Processing Systems Easily

- Achieve highest throughput with enhanced PowerPC 440 processor block
- Accelerate processing performance with custom co-processors
- Increase DSP algorithm performance with built-in DSP48E slices
Reduce Cost through System Integration with Domain-Optimized Platform FPGAs

- Choose a smaller device: 65nm process shrinks die size and new 6-input LUT increases utilization efficiency
- Meet aggressive performance targets in the least expensive speed grade
- Reduce part count with built-in, low-power transceivers
- Increase logic efficiency with built-in PCI Express endpoint and Ethernet MAC blocks
- Integrate embedded processing systems with industry-standard PowerPC 440 processor blocks
- Select smaller heat sinks, fans, and power supplies enabled by reduced power consumption
- Reduce component cost in volume production with Virtex®-5 EasyPath™ FPGAs

Bring Your Product to Market Faster with Proven Development and Verification Tools

- Achieve maximum FPGA performance using ISE® software featuring ISE® software featuring Fmax technology and PlanAhead® design analysis tools
- Design faster and reduce risk with over 125 pre-verified IP cores
- Reach timing closure quickly using new SmartCompile technology that shrinks incremental runtimes
- Optimize designs in less time with SmartPower and ExploreAhead tools that leverage multiple compute platforms
- Speed verification with new FAST simulation models and IEEE IP encrypted models for hard IP
- Reduce debug cycle time with the real-time verification capabilities of ChipScope™ Pro tools
- Implement DSP algorithms modeled using MATLAB® and Simulink® in custom hardware using System Generator for DSP

Finish Your Design Ahead of Schedule with Expert Training and Services

- Ensure your team has all the tools they need with Xilinx Productivity Advantage (XPATM) Program, a bundled solution including software, education, and IP cores
- Accelerate product development with Titanium on-site dedicated engineering from Xilinx
- Ramp your design team with QuickStart, Xilinx professionally delivered training coupled with on-site dedicated engineering
THE ULTIMATE SYSTEM INTEGRATION PLATFORM

65nm ExpressFabric Technology
Achieve highest performance, most efficient utilization on 65nm triple-oxide process
- 30% higher speed, 35% lower dynamic power, and 45% less area than the previous generation
- Industry’s first LUT with six independent inputs for fewer logic levels
- Flexible LUTs are configurable as logic, distributed RAM, or shift registers
- Advanced diagonally symmetric interconnect enables shortest, fastest routing
- From 20,000 to 330,000 logic cells for system-level integration

550 MHz Clocking Technology
Achieve highest speeds with high-precision, low-jitter clocking
- 12 DCMs provide phase control of less than 30 ps for better design margin
- 6 PLLs reduce reference clock jitter by more than 2x
- Differential global clocking ensures low skew and jitter

The Right Memory for Any Application
Distributed RAM—Small
- Build 256-bit memory per CLB
- 64 bits per LUT

550 MHz, 36 Kbit Block RAM—Medium
- Configure Block RAM as multi-rate FIFO
- Built-in ECC for high-reliability systems
- Automatic power conservation circuitry

High-Performance External Memories—Large
- ChipSync™ technology for reliable interfaces
- Achieve data bandwidth up to 389 Gbps
RocketIO GTP Transceivers:
100 Mbps–3.75 Gbps
Implement serial protocols at lowest power
- Flexible SERDES supports multi-rate applications
- Designed to work with integrated PCIe® and Ethernet MAC blocks
- 77% lower power consumption:
  less than 100 mW (typ) at 3.75 Gbps
- Cross-platform pin compatibility makes it easy to migrate to GTX transceivers for design upgrades

RocketIO GTX Transceivers:
150 Mbps–6.5 Gbps
Implement serial protocols at highest line rates
- Flexible SERDES supports multi-rate applications
- Powerful transmit and receive equalization techniques (transmit pre-emphasis, receive linear equalization, and DFE) for best signal integrity at high line rates
- Integrated “gear box” for flexible encoding: 8b/10b, 64b/66b, and 64b/67b
- Designed to work with integrated PCIe and Ethernet MAC blocks
- Low power consumption: less than 200 mW (typ) at 6.5 Gbps

Sparse Chevron Packaging Technology
Keep system noise under control and simplify PCB layout
- Unique PWR/GND pin pattern minimizes crosstalk and reduces PCB layers
- On-substrate bypass capacitors shrink PCB area

Enhanced Configuration and Bitstream Protection
Reduce system cost, increase reliability, and safeguard your design
- Configure with commodity SPI and parallel flash memory
- Easier partial reconfiguration and smaller frame size
- Greater reliability for in-system reconfiguration with multi-bitstream management
- Protect your designs with 256-bit AES (Advanced Encryption Standard) security
**PCI Express Endpoint Block: x1/x4/x8-lane**

Reduce power and cost with built-in support for ubiquitous serial connectivity standard

- Included on PCI-SIG® integrators list after successfully completing the rigorous testing procedures of the Compliance Workshop
- Up to four endpoint blocks in a single Virtex-5 FXT FPGA
- Works with RocketIO GTP/GTX transceivers to deliver full PCIe endpoint function
- Built-in hard IP frees user logic resources and reduces power

**Ethernet Media Access Controller: 10/100/1000 Mbps**

Simplify network connectivity with an integrated tri-mode Ethernet MAC

- UNH-verified compliance
- Up to eight Ethernet MAC blocks in a single device
- Built-in hard IP frees user logic resources and reduces power

**System Monitor and Analog-to-Digital Converter**

Simplify system management and diagnostics

- Fully specified 10-bit, 200k samples/s ADC with programmable monitoring functions (sequencing, averaging, alarms)
- Simplify the implementation and reduce the cost of environmental monitoring
- On-chip temperature and supply voltage sensors
- 17 user-selectable external inputs
- Analog measurements accessible via JTAG at any time
550 MHz DSP48E Slice

Achieve up to 580 GMACS performance using DSP48E slices

- 1,056 DSP48E slices in Virtex-5 SX240T device
- Enhanced slice with a 25x18 multiplier, 48-bit adder, and 48-bit accumulator (cascadable to 96 bits) enables single- and double-precision floating-point and high precision filters with fewer slices
- Configurable for DSP, arithmetic, and bit-wise logic
- Enables efficient adder-chain architectures
- 40% lower power consumption: 1.38mW/100MHz at a 38% toggle rate

1.25 Gbps SelectIO™ Interface with ChipSync Source-Synchronous Technology

Implement industry-standard and custom protocols

- Simplify board design with built-in input delay and new output delay circuits that compensate for unequal trace lengths
- Adaptive delay setting recalibrates automatically to compensate for changing operating conditions
- Interface to popular standards with 1.25 Gbps differential or 800 Mbps single-ended I/O
- Digitally controlled impedance improves signal integrity, reduces component count, and shrinks board size
Simplify Protocol Bridging
Implement Parallel Networking and System Interface Standards
SelectIO technology, combined with pre-verified IP cores, make it easy to support all popular interface standards
• 1.25 Gbps LVDS, 800 Mbps single-ended
• Interface or bridge to virtually any external component
• Support multiple electrical standards in the same device with 35 individually configurable I/O banks
• Design with PCI®, RapidIO, AXI, SPH4.2, and more
• Configure I/Os to support HSTL, LVDS (SDR and DDR), and more, at voltages from 1.2V to 3.3V

Simplify Source-Synchronous Interfacing
ChipSync technology in every SelectIO technology block provides precise control over critical timing for high-performance source-synchronous interfaces
• Achieve performance targets and simplify PCB layout with flexible per-bit deskew
• Synchronize incoming data to FPGA internal clock with built-in Serializer/Deserializer

Build Highest-Bandwidth Memory Interfaces
ChipSync technology and the Memory Interface Generator tool make it easy to build reliable interfaces to the latest high-performance memories, including:

<table>
<thead>
<tr>
<th>Memory Interface</th>
<th>Data Rate (Mbps)</th>
<th>Data Width (# of bits)</th>
<th>Bandwidth (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR SDRAM</td>
<td>600</td>
<td>32</td>
<td>307</td>
</tr>
<tr>
<td>DDR2 SDRAM</td>
<td>667</td>
<td>64</td>
<td>307</td>
</tr>
<tr>
<td>DDR3 SDRAM</td>
<td>800</td>
<td>2 x 32</td>
<td>307</td>
</tr>
<tr>
<td>QDR II SDRAM</td>
<td>600</td>
<td>2 x 324</td>
<td>389</td>
</tr>
<tr>
<td>RLDRAM II</td>
<td>600</td>
<td>648</td>
<td>389</td>
</tr>
</tbody>
</table>
Create Highest-Performance DSP Systems

Increase DSP algorithm performance
- Build single or multi-rate filters for high-sample-rate applications in wireless RF or HD video systems with cascadable DSP48E slices
- Perform fine-granularity data shifting, control, and small bit-width arithmetic functions efficiently in programmable logic fabric
- Free up DSP processor CPU cycles by off-loading algorithm-intensive tasks to the FPGA co-processor
- Obtain highest memory-to-logic ratio with Virtex-5 SXT platform for efficiently implementing memory-intensive functions in video processing and medical imaging

Optimize DSP power consumption and cost
- Achieve efficient implementation with Xilinx algorithm/IP core support for base functions (e.g. FFT filters), wireless functions (e.g. DDC, DUC, CFR, DPD) or video/imaging functions (e.g. CODECs)
- Use power-efficient Virtex-5 FPGAs in military manpack or handheld software defined radios

Build flexible, high-bandwidth interfaces
- Simplify design with built-in support for PCI Express interfaces
- Obtain complete Xilinx solutions for market-specific interfaces such as CPRI™ and OBSAI for wireless or SDI and HD-SDI for professional broadcast systems
- Build high-bandwidth interfaces to DSP processors using Xilinx IP and reference designs for serial RapidIO, VHYDRO™ interface products, or EMIF interfaces when using FPGAs as DSP co-processors

Increase DSP Design Productivity
- Develop DSP custom hardware using MATLAB and Simulink design environments
- Accelerate DSP system verification up to 1000x using hardware co-simulation
- Gain immediate FPGA expertise from a Xilinx application specific on-site engineer, improving your design productivity and accelerating your time-to-market with Titanium Dedicated Engineering.

Build SoC Designs with High-Performance Embedded Processing

Create customized embedded systems that meet your unique and exacting requirements
- Integrate high-speed programmable logic with the flexibility of software to optimize performance, power, and cost
- Design system-on-chip functionality with real-time processing capabilities using processor blocks incorporating industry-standard PowerPC 440 processor cores built into Virtex-5 XTX devices
- Implement control functions efficiently in all Virtex-5 FPGAs using MicroBlaze™ soft processors

Achieve highest throughput with enhanced PowerPC 440 processor blocks
- Get non-blocking pipelined point-to-point access to TEMAC, PCIe blocks, and FPGA logic
- Offload PLB with a dedicated memory interface port that provides up to 128-bit data transfer per cycle
- Maximize data transfer rates with highly pipelined transmit and receive scatter/gather DMA channels
- Optimize system performance through user-selectable port prioritization and operating frequencies

Accelerate system performance
- Offload CPU-intensive operations such as video processing, 3D data processing, and floating-point math
- Create custom co-processors in the FPGA logic
- Optimize hardware/software partitioning with the PowerPC 440 processor block Auxiliary Processor Unit (APU) controller
- Implement double/single-precision arithmetic operations using IEEE 754-compatible Floating Point Unit option

Streamline Embedded Development and Empower Innovation
- Accelerate processing design with the award winning Platform Studio tool suite
- Increase productivity with design wizards, customizable IP, and integrated HW/SW kits
- Simplify system-level debugging using Eclipse SDK and ChipScope Pro integrated bus analyzer
- Leverage broad ecosystem support from industry leaders in real-time OS, design, debug, and trace technologies
- Provide your team with expert advice and training at the most critical project stage with QuickStart for Embedded designs

FOR EVERY PLATFORM

Create highest-performance DSP systems with Virtex-5 FXP FPGAs.
Implement PCI Express Technology with Reduced Cost, Power, and Complexity

Minimize design risk with hardened PCIe blocks for building next-generation graphics, storage, networking, and I/O devices

- Integrate multiple functions into a single PCIe technology-enabled FPGA
- Preserve software investment and extend infrastructure life with scalable bandwidth (x1, x4, x8)
- Re-target designs without changing your PCIe interface implementation as your project evolves
- Experience a shorter development cycle with QuickStart! for PCIe designs: an on-site Xilinx dedicated engineer will assist your team with expert advice and training

Accelerate development with ready-to-use solution kits

- Protocol compliance reports
- Device characterization
- Reference designs
- Development boards
- Simulation models
- Pre-verified IP
- Development tools
- User documentation
- Partner solutions

Application of PCI Express Technology in a Server System
### Virtex-5 Family

**Part Number**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>CLB Flip-Flops</th>
<th>DSP48E Slices</th>
<th>I/O Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF324</td>
<td>19,200</td>
<td>360 (8)</td>
<td>640 (16)</td>
</tr>
<tr>
<td>FF676</td>
<td>38,720</td>
<td>640 (16)</td>
<td>680 (16)</td>
</tr>
<tr>
<td>FF1153</td>
<td>79,200</td>
<td>800 (800)</td>
<td>800 (800)</td>
</tr>
<tr>
<td>FF1760</td>
<td>14,512</td>
<td>800 (800)</td>
<td>800 (800)</td>
</tr>
</tbody>
</table>

**I/O Resources**

<table>
<thead>
<tr>
<th>Package</th>
<th>Area</th>
<th>19,200</th>
<th>220</th>
<th>220</th>
<th>220</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF324</td>
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<td></td>
</tr>
</tbody>
</table>

**Clock Resources**

<table>
<thead>
<tr>
<th>Speed Grades</th>
<th>Commercial</th>
<th>Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
</tr>
<tr>
<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
</tr>
<tr>
<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
</tr>
<tr>
<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
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<td>-1,-2</td>
<td>-1,-2</td>
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<tr>
<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
</tr>
<tr>
<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
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<td></td>
<td>-1,-2</td>
<td>-1,-2</td>
</tr>
</tbody>
</table>

**Configuration Memory (Kbits)**

| Configuration Memory (Kbits) | 8.4 | 12.6 | 21.9 | 29.2 | 41.1 | 53.2 | 79.8 | 640 (16) |

**Notes**

1. EPLD solutions provide a convenient path for volume production.
2. An angelstrom FPGP CLB contains two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in Virtex-4 FPGA slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
3. A single Virtex-5 FPGA CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in Virtex-4 FPGA slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
4. There is a 64-kbit EPLD logic cell array that reflects the increased logic capacity offered by the new 64-kbit EPLD architecture.
5. A single Virtex-5 FPGA CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in Virtex-4 FPGA slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
6. PowerPC 440 Processor Blocks
7. FPGA Express SRAM Blocks
8. 1Gb/2Gb/4Gb Ethernet MAC Blocks
9. RocketIO GTX High-Speed Transceivers
10. RocketIO GTP Low Power Transceivers

**EasyPath Cool Reduction Solutions**

| Configuration Memory (Kbits) | 8.4 | 12.6 | 21.9 | 29.2 | 41.1 | 53.2 | 79.8 | 640 (16) |

**Logic Resources**

<table>
<thead>
<tr>
<th>Logic Resources</th>
<th>Logic Cells</th>
<th>CBR</th>
<th>GBR</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF324</td>
<td>32</td>
<td>48</td>
<td>64</td>
</tr>
<tr>
<td>FF676</td>
<td>40</td>
<td>440</td>
<td>440</td>
</tr>
<tr>
<td>FF1153</td>
<td>50</td>
<td>560</td>
<td>560</td>
</tr>
<tr>
<td>FF1760</td>
<td>64</td>
<td>640</td>
<td>640</td>
</tr>
</tbody>
</table>

**Embedded Hard IP Resources**

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<tr>
<th>Embedded Hard IP Resources</th>
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<th>FPGA Express SRAM Blocks</th>
<th>1Gb/2Gb/4Gb Ethernet MAC Blocks</th>
<th>RocketIO GTX High-Speed Transceivers</th>
<th>RocketIO GTP Low Power Transceivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF324</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>FF676</td>
<td>4</td>
<td>1</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>FF1153</td>
<td>6</td>
<td>1</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>FF1760</td>
<td>8</td>
<td>1</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

**Configuration Memory (Mbit)**

| Configuration Memory (Mbit) | 8.4 | 12.6 | 21.9 | 29.2 | 41.1 | 53.2 | 79.8 | 640 (16) |

**PowerPC 440 Processor Blocks**

<table>
<thead>
<tr>
<th>PowerPC 440 Processor Blocks</th>
<th>2</th>
</tr>
</thead>
</table>

**FPGA Express SRAM Blocks**

<table>
<thead>
<tr>
<th>FPGA Express SRAM Blocks</th>
<th>1</th>
</tr>
</thead>
</table>

**1Gb/2Gb/4Gb Ethernet MAC Blocks**

<table>
<thead>
<tr>
<th>1Gb/2Gb/4Gb Ethernet MAC Blocks</th>
<th>2</th>
</tr>
</thead>
</table>

**RocketIO GTX High-Speed Transceivers**

<table>
<thead>
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<th>RocketIO GTX High-Speed Transceivers</th>
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</tr>
</thead>
</table>

**RocketIO GTP Low Power Transceivers**

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<th>RocketIO GTP Low Power Transceivers</th>
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</tr>
</thead>
</table>
Footprint Compatible Packaging Enables Design Flexibility

Devices in the same package type are footprint compatible for easy migration across densities and platforms. You can accommodate changing requirements or implement system upgrades by moving your design to another pin-compatible device offering a different mix of capabilities, speed, or processing power, without changing your board layout.