

# AES Audio Transmitter & Receiver Reference Designs for Xilinx FPGAs



## Industry challenges

- Support industry standard interfaces for high-end audio and video applications
- Differentiation of products through extra features or reduced cost

## Xilinx Solutions

- Free-of-charge reference designs for audio Tx and Rx
- Easy to integrate into your own FPGA designs
- Reduce or remove cost of external audio ASSPs

## Complete reference designs available for quick and easy design

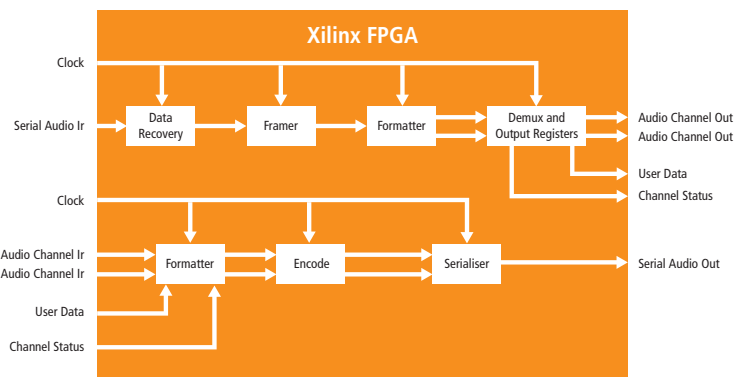
Xilinx AES audio reference designs enable hardware engineers to easily integrate industry standard interfaces into their products using FPGAs as a cost-effective and flexible alternative to application specific standard products (ASSPs). This allows them to concentrate on the value-add portion of their designs. They also enable current Xilinx FPGA users to remove the need for separate components to perform these tasks, resulting in more complete system-on-chip designs.

## Add differentiating features to your product while saving costs

Implementing these readily available interfaces on a system-level Xilinx FPGA eliminates the costs associated with external components, including external devices and the hidden costs related to PCB requirements. Further major benefits of FPGA implementation include the ability to adapt interfaces to meet your specific needs, the addition of extra processing tasks, and support for multiple channels in a single device.

## Reference Design Specifications and FPGA Resources

Standards supported:	AES3-2003	Channel status supported:	✓
	SMPTE 337	Channel status supported:	✓
	S/PDIF	User data supported:	✓
Audio sample rates:	Any	Application note:	XAPP514
Bits per audio sample:	Up to 24	Source code:	VHDL & Verilog



AES Tx and Rx Example

Function	LUTs	FFs	Virtex-4	Virtex-II Pro	Spartan-3E	Spartan-3
AES3	100	50	✓	✓	✓	✓
AES3	115	205	✓	✓	✓	✓

## Single Reference Clock

The receiver uses digital over-sampling to recover the serial data. No PLLs are required.

A single reference clock is needed for all AES3 receivers in the FPGA. Given a sufficiently fast reference clock, the receiver can support any AES3 audio sample rate. Xilinx recommends a minimum reference clock frequency of 100 MHz to support all AES3 sample rates up to 192 kHz. The reference clock can be generated by a DCM from a lower frequency clock source.

## Supports All AES3 Information

The receiver captures all information in the AES3 signal and makes it available to the application. This includes channel status and user data, and verification of channel status CRC. The transmitter also supports any AES3 sample rate. Channel status and user data information are inserted into the signal. Channel status CRC can be calculated and inserted into the signal.

## Take the Next Step

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