Audio Sample Rate Converter Reference Design for Xilinx FPGAs

Industry challenges

- Be able to handle any audio frequency in-and-out
- Maintain highest audio quality while remaining cost competitive

Xilinx Solutions

- Free-of-charge reference designs for audio SRC
- -130dB THD+N typical
- Supports 8kHz to 192kHz
- Input/output ratios 8:1 to 1:7.5
- Easy to integrate into your own FPGA system designs
- Reduce or remove cost of external audio ASSPs

High quality asynchronous sample rate converter with ultimate flexibility

Audio applications require different sampling frequencies depending on the sources and destinations of the audio streams. Source material recorded with one sample rate often must be converted to another sample rate for processing. The asynchronous sample rate converter reference design addresses these conversion requirements by leveraging the unrivalled DSP horsepower of Xilinx FPGAs.

Ideal for a wide range of markets and applications

Implementing the sample rate converter on a Xilinx FPGA offers a low-cost alternative to standard products that can be easily integrated into system-on-chip designs. The flexible and reprogrammable nature of Xilinx devices enables you to configure and adapt the SRC to meet the specific needs of your application.

Unlike a standard off-the-shelf device, complete programmability also offers the ability to include additional interfaces or further audio, video or system processing tasks, or even support for many channels in a single device. Applications range from professional audio and broadcast equipment, to consumer and in-car audio systems.

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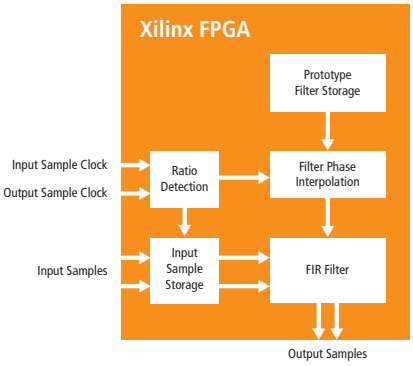
Reference Design Specifications and FPGA Resources

Input rates:	8 kHz to 192 kHz	Fully asynchronous:	✔
Output rates:	8 kHz to 192 kHz	Automatic ratio detection:	✔
Up conversion:	8:1 continuous	Rate change tracking:	✔
Down conversion:	1:7.5 continuous	Deterministic latency:	✔
Audio word width:	24 bits In & Out	Sample clock jitter rejection:	✔
Performance:	-130db THD + N	Lock status for external mute:	✔
		1:1 asynchronous conversion:	✔
		Applicaton note:	XAPP514
		Source code:	VHDL & Verilog



Sample Rate Converter Example

Function	LUTs	FFs	Virtex-4	Virtex-II Pro	Spartan-3E	Spartan-3
Audio SRC	2750	3235	✓	✓	✓	✓

Sample Rate Converter Overview and Operation

The asynchronous sample rate converter converts stereo audio from one sample frequency to another. The input and output sample frequencies may be an arbitrary fraction of one, or another or the same frequency, but based on different clocks.

The output is a band-limited version of the input, re-sampled to match the output sample timing. The ratio detection logic tracks input and output frequencies. Relative phase of the input to output samples is calculated to extremely high accuracy. Based on this phase, a set of filter co-efficients is interpolated from the stored prototype low- pass filter. These co-efficients are applied as a FIR filter to the corresponding set of input samples from the input sample storage to obtain the converted output sample. The SRC retains full performance over the AES3-2003 jitter tolerance curve.

Take the Next Step

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