Spartan-3 Generation FPGAs – The Ultimate Low-Cost Applications Platform





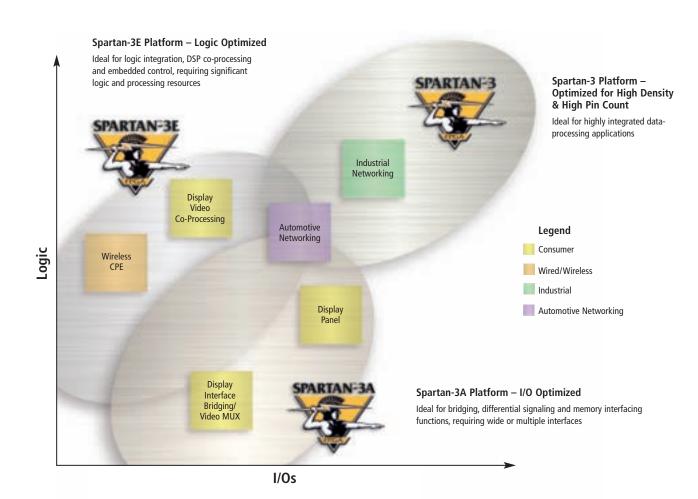


FPGAs FOR VOLUME APPLICATIONS

One Generation – Multiple Domain-Optimized Platforms

With the introduction of the new Spartan[™]-3A platform, the Spartan-3 Generation of FPGAs now offers a choice of three platforms, each delivering a unique cost-optimized balance of programmable logic, connectivity, and dedicated hard IP for your low-cost applications. The new Spartan-3A FPGAs are optimized for applications emphasizing I/O count and capabilities, and complement the existing Spartan-3E and Spartan-3 platforms.

Spartan-3 Generation FPGAs utilize the industry's most cost-effective and production-proven process technology — with over 25 million devices already shipped to thousands of customers worldwide.



Flexibility and Low Cost — The Ultimate Choice for Volume Applications

Systems designers worldwide are leveraging the unique advantages of Spartan-3 Generation FPGAs across a wide range of end applications, adapting their products to rapidly changing interface and data standards, differentiating functionality with minimum design time, and reducing risk as they ramp to higher production volumes.

Examples	Application Challenges	Spartan-3 Generation Advantages							
Flat Panel Displays	 Panel board and video/tuner board cost Constantly evolving I/O requirements Shorter product life cycles with higher amortized cost risk for new ASICs Constantly evolving, subjective image quality requirements Differentiating vs. competing hardware 	 3 domain-optimized platforms for lowest-cost fit to each application SelectIO™ Technology with on-chip differential termination and widest I/O standards compliance, including LVDS, RSDS, mini-LVDS, PPDS and TMDS Pre- or post-processing video enhancement, LVDS TxRx (FPDLink), and peripheral interface bridging solutions TCON (timing control) and video co-processing flexibility Flexible peripheral interfacing and video switching Reference designs for precise gamma correction, image dithering, color temperature correction and other video-enhancement functions 							
Set-Top Boxes	 Evolving interface standards for memory, disks, and other components Managing inventory with multiple product feature sets Differentiating video processing capability at lower power and cost Accelerating and updating algorithms for conditional access/security 	 SelectIO Technology with support for up to 26 different I/O standards Multi-boot reconfigurability and density migration within a single package XtremeDSP™ Technology with industry-leading price/performance for digital video decoding Fast, compact IP cores for authentication and content encryption 							
Wireless Access	 Low-level MAC-layer co-processing in Customer Premises Equipment Forward Error Correction and DSP co-processing efficiency Peripheral bridging and interfacing 	 IP cores for MAC, FEC, encryption, digital up/down conversion and security XtremeDSP Technology with flexible high performance SelectIO Technology with on-chip termination and wide I/O standards support 							
Industrial Ethernet and Motion Control	 Bridging multiple connectivity protocols Customizing PWM and control algorithms Accelerating motion control algorithms 	 IP cores for EtherCAT, SerCOS III, CAN, Ethernet, PCI and PCI Express Flexible Xilinx Embedded Processing Technology Hardware acceleration with Fast Simplex Link and XtremeDSP Technology 							
Automotive	 Full compliance to industry production process and quality standards Interconnecting different automotive/multimedia standards 	 Extended Automotive temperature ranges, both Industrial and Q-Grade; full PPAP support and AEC-Q100 qualification for Spartan-3 and Spartan-3E platforms IP cores for bridging CAN, LIN and MOST as well as USB 2.0 and Ethernet XtremeDSP Technology with industry-leading price/performance/power and IP for filtering, edge detection, and codes Select IO Technology with on-chip termination for LVDS, RSDS and other standards 							



THE ULTIMATE LOW-COST APPLICATIONS PLATFORM

The Lowest-Cost Programmable Logic Platform

Integrate system functions more efficiently

- Sophisticated clock management offers increased flexibility and control for high-performance systems
- Embedded 18 Kbit dual-port RAM blocks provide efficient processor code and data storage
- Embedded 18 x 18 multipliers deliver high-performance DSP
- Distributed RAM and shift registers for smallest design footprint

Flexible Power Management*

Reduce system power consumption

- Suspend mode reduces total FPGA power more than 40%
- Hibernate mode reduces quiescent power up to 98%





Robust Anti-Cloning Security*

Prevent design cloning and unauthorized overbuilding

- Every device has a unique Device DNA serial number for userdefined authentication
- Ultimate flexibility with user-defined authorization for both hardware and critical software IP

The Most Comprehensive Configuration Capabilities

Reduce system cost, boot with different functions, and upgrade reliably

- Broadest flash memory support for lowest-cost configuration, including Platform Flash and commodity serial (SPI) and parallel flash memories
- Multi-Boot capability for multiple system configurations from the same hardware



The Leading Connectivity Platform

Implement multiple bridging, differential signaling and memory interfaces with SelectIO™ Technology

- Supports most popular and emerging single-ended and differential signaling standards including TMDS, PPDS, SSTL3 Class I & II *
- Pre-engineered interface IP solutions including PCI, PCI Express, USB, Firewire, CAN, SPI, I2C, and more
- Full hot-swap compliance and 3.3V support *

The Most Extensive Package Options

Select plastic to ceramic, smallest (8x8 mm² CP132) to largest (FG1156)



• Pb-free availability for all packages



8x8 mm2 CP132

Valid Data Lines Calibration Clock

The Best Design Margins with Low-Cost Source Synchronous Interfacing Technology*

Ensure reliable data-clock synchronization

- Dynamic Input Delay technology with real-time flexibility
- Simplifies DDR and DDR2 memory interface design

Platform	Cost-Optimization	Ideal Applications	Logic Cells	I/Os	Security	Power Management	SelectIO [™] Technology	DSP Resources	Configuration
Spartan-3A	I/O count & capabilities	Wide or multiple interfaces – bridging, differential signaling, memory interfaces	1584 to 25,344	108 to 502	Internal with Device DNA	Suspend—more than 40% reduction Hibernate—up to 98% reduction XPower Analyzer tools	Supports 26 differential and single-ended I/O standards Enhanced differential signaling with on-chip input termination TMDS, PPDS, RSDS, LVDS, DDR, DDR2 and SSTL3 class I & II Full 3.3V and hot-swap compliance	Pipelined, embedded 18 x 18 multipliers 18 Kbit dual-port RAM Distributed RAM and shift registers	Platform Flash with full support Parallel flash with Multi-Boot plus watchdog SPI flash JTAG and full ISE™ tool support
Spartan-3E	Logic density	Lowest-cost logic density—logic integration, DSP co-processing, embedded control	2160 to 33,192	66 to 376	External with SHA PROM	XPower Estimator and XPower Analyzer tools	Supports 18 differential and single-ended I/O standards Up to 16mA drive DDR memory interfaces	Pipelined, embedded 18 x 18 multipliers 18 Kbit dual-port RAM Distributed RAM and shift registers	Platform Flash with full support Parallel flash with Multi-Boot SPI flash; JTAG and full ISE tool support
Spartan-3	High logic density and I/O count	High logic and I/O densities—highly integrated data-processing	Up to 74,880	Up to 784	External with SHA PROM	XPower Analyzer and Web Power tools	Supports 24 differential and single-ended I/O standards Up to 24mA drive DDR and DDR2 memory interfaces	Embedded 18 x 18 multipliers 18 Kbit dual-port RAM Distributed RAM and shift registers	Platform Flash, with easy in-system reprogrammability, compression, JTAG and full ISE tool support

FAST, FLEXIBLE SYSTEM

Implement Customizable Lowest-Cost Networking and System Interfaces

Optimized silicon and application-specific IP cores make it easy to support all popular low-cost interface standards.

PCI Express

- Fully-compliant to PCIe-Base Specification v1.1 specifications
- PCI Express Starter Kit, including development board
- PCI Express PIPE Endpoint LogiCORE™ IP
- Reference Design with third-party PHY
- Bundled solution pricing



PCI 33 and 66MHz, fully PCI 3.0-compliant

- PCI32 and PCI64 LogiCORE IP cores
- Customizable back-end functionality

Ethernet

- Designed to the IEEE 802.3-2002 specification for 1000 Mbps, 100 Mbps, and 10 Mbps modes
- Customizable LogiCORE Tri-Mode Ethernet MAC
- Integrates with the Ethernet 1000BASE-X PCS/PMA or SGMII LogiCORE for implementation of Ethernet Link and Physical layers



SPI-4.2, functionally compliant with OIF and SATURN® specifications

 SPI4.2(PL4) Lite LogiCORE™ delivers Sink and Source cores selected and configured through Xilinx CORE Generator™

CAN, designed to ISO 11898-1, CAN2.0A and CAN2.0B specifications

- User-configurable CAN LogiCORE IP
- Stand-alone mode or connected to Xilinx MicroBlaze[™] processor

INTEGRATION

Integrate Soft Embedded Processors

Xilinx offers flexible programmable processing solutions and a unified development tool suite

- Customizable 32-bit MicroBlaze soft processor with a full set of peripherals and reference designs
- No risk of processor or code obsolescence
- Flexibility to perform rapid design updates and changes
- Embedded Development Kit and award-winning Platform Studio tool suite
- Small-footprint PicoBlaze[™] 8-bit processing solution for assemblyprogrammed applications

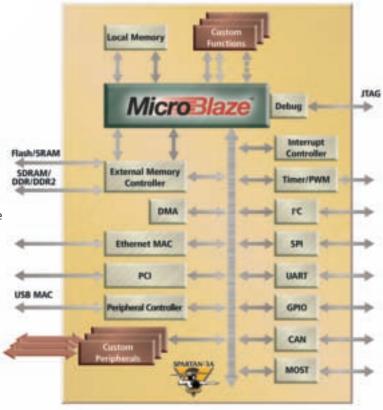
Accelerate DSP Algorithms Efficiently

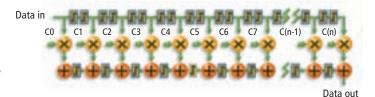
Spartan-3 Generation FPGAs offer the best DSP price/power/performance for cost-conscious applications. Optimized silicon advantages including embedded multipliers, block RAM, distributed RAM and SRL16 shift registers, AccelDSP™ and System Generator for DSP tools, plus pre-verified IP cores make Spartan-3 Generation solutions ideal for:

 Video: H.264 decoding, compression, color space conversion, warping, rotation, scaling, and edge detection



- Multi-channel Audio: noise reduction, modulation and demodulation, encoding and decoding
- Communications: sample-rate conversion, filtering, down- and upconversion, modulation and demodulation, forward error correction, encryption, compression, signal conditioning (filtering and stabilization), and decimation





Build Memory Interfaces Quickly and Reliably

Dynamic Input Delay Technology and the Memory Interface Generator tool make it easy to build reliable interfaces to the latest low-cost memories, including DDR2 and DDR

Memory Device	Electrical Interface	Clock Rate	Data Rate		
DDR2 SDRAM	SSTL 1.8V	166 MHz	333 Mbps		
DDR SDRAM	SSTL 2.5V	166 MHz	333 Mbps		

Finish Your Design Ahead of Schedule

- Achieve FPGA performance goals quickly with ISE™ Fmax technology and PlanAhead™ design analysis tools
- Reduce debug cycle time with the real-time verification capabilities of ChipScope™ Pro tools
- Accelerate product development with online resources, training courses, and premium support services
- Get Xilinx Productivity Advantage (XPA) bundles of software, education, support services, and IP cores
- Augment your development team with a worldwide network of Xilinx
 Design Service (XDS) and partner experts

	Spartan-3 Optimized for High Density and High I/O Designs						Spartan-3E Logic optimized				Spartan-3A I/O optimized							
Part Number	XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000	XC3S100E	XC3S250E	XC3S500E	XC3S1200E	XC3S1600E	XC3S50A	XC3S200A	XC3S400A	XC3S700A	XC3S1400A
System Gates	50K	200K	400K	1000K	1500K	2000K	4000K	5000K	100K	250K	500K	1,200K	1,600K	50K	200K	400K	700K	1400K
Logic Cells	1,728	4,320	8,064	17,280	29,952	46,080	62,208	74,880	2,160	5,508	10,476	19,512	33,192	1,584	4,032	8,064	13,248	25,344
Dedicated Multipliers	4	12	16	24	32	40	96	104	4	12	20	28	36	3	16	20	20	32
Block RAM Blocks	4	12	16	24	32	40	96	104	4	12	20	28	36	3	16	20	20	32
Block RAM Bits	72K	216K	288K	432K	576K	720K	1,728K	1,872K	72K	216K	360K	504K	648K	54K	288K	360K	360K	576K
Distributed RAM Bits	12K	30K	56K	120K	208K	320K	432K	520K	15K	38K	73K	136K	231K	11K	28K	56K	92K	176K
DCMs	2	4	4	4	4	4	4	4	2	4	4	8	8	2	4	4	8	8
Max Single Ended I/O	124	173	264	391	487	565	712	784	108	172	232	304	376	144	248	311	372	502
Max Diff. I/O Pairs	56	76	116	175	221	270	312	344	40	68	92	124	156	52	112	142	165	227
VQ100 16 x 16 mm	63	63							66	66								
CP132 8 x 8 mm	89								83	92	92							
TQ144 22 x 22 mm	97	97	97						108	108				108				
PQ208 30.6 x 30.6 mm	124	141	141							158	158							
FT256 17 x 17 mm		173	173	173						172	190	190		144	195	195		
FG320 19 x 19 mm			221	221	221						232	250	250		248	251		
FG400 21 x 21 mm												304	304			311	311	
FG456 23 x 23 mm			264	333	333	333												
FG484 23 x 23 mm													376				372	375
FG676 27 x 27 mm				391	487	489	489											502
FG900 31 x 31 mm						565	633	633										
FG1156 35 x 35 mm							712	784										

Note: 1. System Gates include 20-30% of CLBs used as RAMs.

2. Numbers in table across device packages indicate maximum number of user I/Os.



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