

Xilinx Solutions for PCI Express Made Easy



PCI Express Design Challenges

- Scaling performance to meet changing requirements
- Building systems for smaller form factors and stringent power budgets, at lower costs
- Getting to market faster with proven interoperability and lowest risk

Xilinx PCI Express Solutions

- Ultimate flexibility and fast time-to-market
- Virtex-5 FPGAs with multiple built-in IP blocks provide a high-performance, scalable and low power solution for multilane PCIe applications
- Optional Soft-IP for Virtex-series FPGAs
- Spartan-3 generation FPGAs plus external PHYs provide a low-cost solution

Xilinx helps you implement PCI Express® designs in the shortest possible time with easy-to-use 1-8 lane solutions that meet performance, power and cost targets.

Virtex-5

Future-proof your Application with Scalable Performance

With built-in transceivers and multiple endpoint blocks to support PCIe® in Virtex-5 platform, you can easily scale from 1-8 lanes and migrate from the Gen1 to Gen2 specification. Design for today and tomorrow with cross-platform pin compatibility.

Reduce Power with Built-in Blocks for PCIe

65nm Virtex-5 FPGAs with built-in, power optimized RocketIO GTP transceivers, high performance RocketIO GTX transceivers and multiple built-in endpoint blocks for PCIe ensures implementations to target lowest power consumption or highest bandwidth solutions.

Spartan-3

Lower Cost for a Wide Range of Applications

Spartan-3 generation FPGAs with soft endpoint IP for PCIe and external PHY provide the lowest cost programmable PCIe solution for consumer and other high-volume applications.

Reduce Risk with Proven Compliance & Protocol Characterization

Xilinx solutions for PCIe are certified at PCI-SIG workshops (see Integrator's List) and characterized across process, voltage, and temperature.

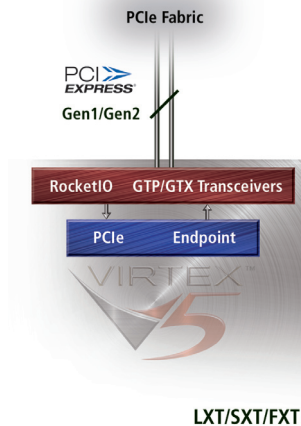
Finish Faster with Easy-to-Use Development Kits

Xilinx development kits include hardware verified IP, tools, reference designs, and development boards to help you reduce design time by >50%.

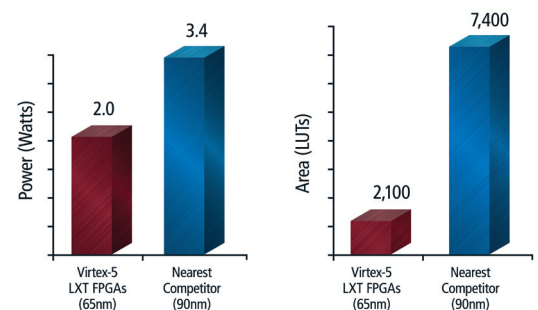
High Performance Solutions for PCI Express – Virtex FPGAs

Virtex-5 LXT/SXT/FXT

- Built-in solution:
 - V5 LXT/SXT: x1-x8 PCIe Endpoint block and low-power GTP transceivers
 - V5 FXT: up to four x1-x8 PCIe Endpoint blocks and high-performance GTX transceivers for PCIe v2.0 support (“Gen2”)
- Hardware verified to PCIe Base Specification v1.1
- Multi-vector MSI and INTx emulation
- Up to 512 byte maximum payload size (MPS)
- Configurable BARs for memory or I/O
- Compliant with PCI / PCI Express power management functions
- IP delivered through CORE Generator using built-in PCIe blocks and transceivers

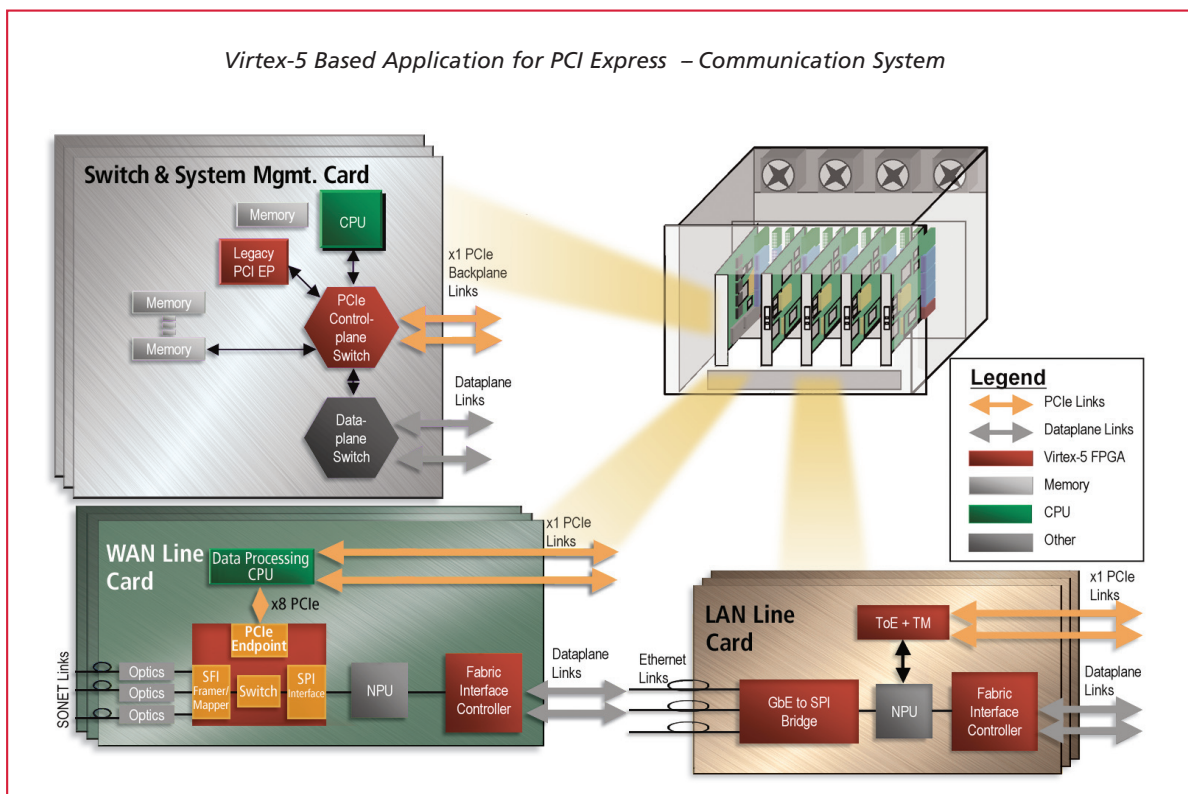


Power consumption and logic resources required to implement an 8-lane PCIe endpoint



5VLX30T vs. 2SGX60D: the smallest devices available from each vendor capable of implementing a x8 PCIe Express interfaces.
Power consumption estimates from Xilinx tool v9.2 and competitor tool v7.2 SPI

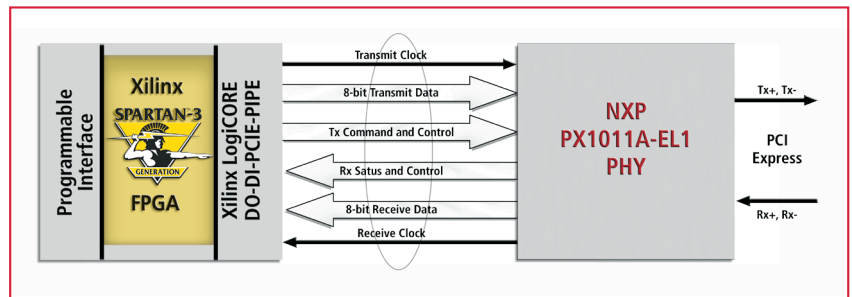
Virtex-5 Based Application for PCI Express – Communication System



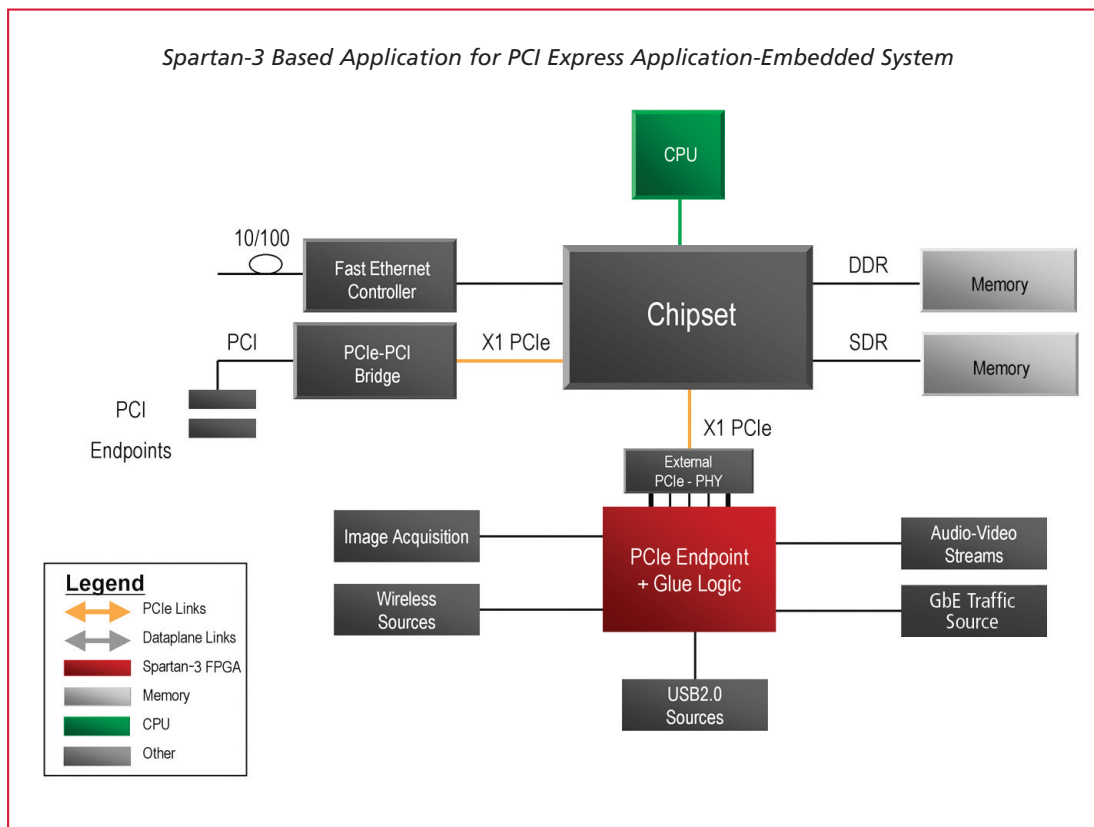
Low Cost Solutions for PCI Express – Spartan FPGAs

Spartan-3 Generation

- x1 PCIe Endpoint soft IP with external PHY
- Compliant to PCIe Base Specification v1.1
- MSI and INTx emulation and configurable BARs for memory or I/O
- 512 bytes maximum payload size (MPS), 1VC, power management
- Delivered through CORE Generator as configurable IP with PIPE interface



Spartan-3 Based Application for PCI Express Application-Embedded System



PCI Express Development Kits

Virtex-5 Edition



MSRP: \$2200

Spartan-3 Edition



MSRP: \$349

Development Kits include:

- Development Board
- Download Cable
- Software (60 day eval)
- LogiCORE IP
- Reference Designs
- Drivers and GUI
- Quick start guide (Multi-Lingual)
- Tech Docs and Collateral

Learn more about Xilinx Solutions for PCI Express

- Demo-on-Demand
- Techonline webcast
- Sign up for a 2-day class
- Order a development kit
- Call your Xilinx sales representative for a demo
- Contact platformsteam@xilinx.com

TAKE THE NEXT STEP

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