REDUCE CAPEX AND OPEX
WITH DIGITAL PRE-DISTORTION

Digital Pre-Distortion

As cellular infrastructure equipment evolves, greater demands are placed on the transmission and reception systems employed within basestations. Increasing data rates are driving the need for improved spectral efficiency, through the use of higher order modulation schemes, where increased Bits/s/Hz performance results in better use of existing spectrum. The side effect of many of these newer transmission systems, is that they require very high linearity performance from the Power Amplifier (PA) modules.

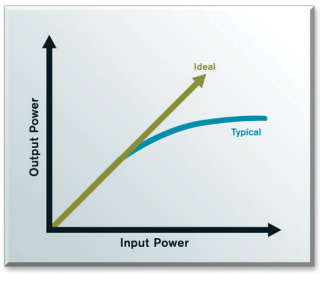
To ensure that the transmission of the intended spectrum doesn't violate the standard's spectral mask, the PA must be backed off to run in its linear region. This results in minimal signal distortion prior to transmission. The by-product is however, low efficiency; typically around 10% for Class AB amplifiers with no Digital Pre-Distortion (DPD).

It is widely recognized that the PA modules contribute to significant running costs of basestations due to their poor efficiency. As a result, DPD can be used to extend the linear range of PAs, resulting in far higher efficiency and reduced operational costs.

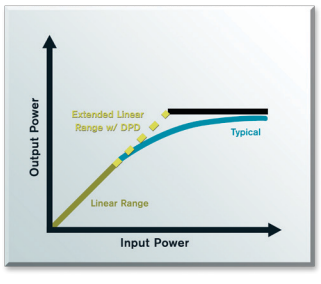
Xilinx Digital Pre-Distortion (DPD) Reference Design

The Xilinx Digital Pre-Distortion reference design uses a combination of high-speed data path processing and software running on a MicroBlaze™ processor. The processor subsystem is used to calculate sets of values that represent the behavior of the amplifier under certain signal conditions. These values are then used to precondition the signal before it enters the PA. Tests have shown the efficiency achieved with the Xilinx DPD design, on a typical Class AB power amplifier module, approaches thirty-seven percent - which is a significant improvement from the ten percent range. The end result of this enhancement, when applied to typical network deployment, leads to millions of dollars saved per annum in operational expenditure.

DIGITAL CORRECTION OF AMPLIFIER NON-LINEAR REGION



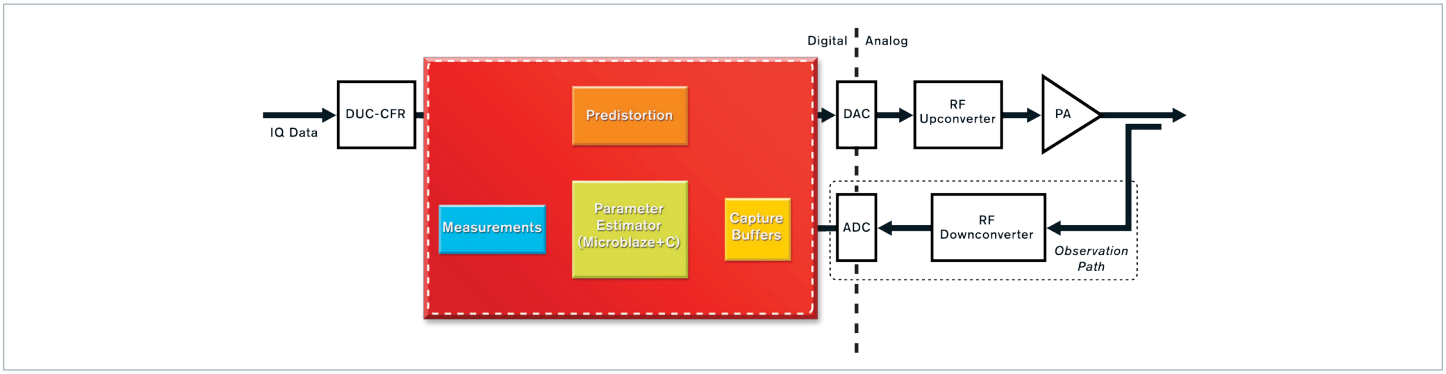
PA Behavior Prior to DPD Processing.



Digital correction of amplifier non-linear region, allowing back off level reduction and increased output power.

XILINX®

XILINX DIGITAL PRE-DISTORTION SOLUTION



DPD V2.0 Features

- Support for Xilinx Virtex®-4 and Virtex®-5 devices
- Single and dual antenna versions available
- Low utilization

DESIGN	LOGIC SLICES*	DSP48S	BRAM*
Virtex-4, 1Tx	2826	19	60
Virtex-4, 2Tx	3757	31	69
Virtex-5, 1Tx	1604	19	32
Virtex-5, 2Tx	1881	31	36

* Virtex-4 device logic slice architecture and BRAM depth is different than Virtex-5 devices

- Low power – 800mW (1Tx) and 1.2W (2Tx) typical measured dynamic power
- High performance – spectral correction ranging from 15-30dB depending on amplifier and air interface
- Transmit bandwidth – 15MHz+ (Virtex-4 FPGA), 20MHz+ (Virtex-5 FPGA)
- Support for up to 20MHz+ transmit bandwidth
- Support for memory and reactive effects
- Overdrive detection and adaptive Quadrature Modulation Correction (QMC)
- Tested with 30+ power amplifiers ranging from Class AB to symmetric/asymmetric doherty architectures and extensive testing with Freescale HV7/HV8 generation transistors
- Tested with existing Xilinx Digital Front End reference designs on the AXIS CDRSX(2) radio development board covering GSM, CDMA2000, WCDMA, WiMAX, LTE and TD-SCDMA

Availability

The Xilinx DPD design is available now for Virtex-4 and Virtex-5 FPGAs.

To request your copy of the DPD reference design please contact your local Xilinx sales representative.

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