DESIGN TOOL QUALITY

Vivado™ Surpasses Quality Records

A number of architecture, process, test, and development improvements were implemented during 2012 to meet increasing customer expectations with the Xilinx design tool suites, ISE® and Vivado. The main priority was to increase the effectiveness of testing to find and fix more issues earlier. This initiative has yielded significant benefits during customers' product development life cycles:

- *Fewer respins of new features and less time lost reworking old code*
- *More developer time for feature development and algorithm tuning*
- *More testing time for complex designs and new user flows*

CASE STUDIES

To achieve these results, Xilinx carried out:

- *Additional nightly test cycles for better regression and testing*
- *Regression testing with 2.6x more complex designs*
- *More pre-commit checks (with IP subsystem tests added) for stronger IP error checks*

How have these advances measurably improved Xilinx product quality? Three key metrics demonstrate these gains:

1. **Downward trend for customer-found high-priority change requests (CRs).** (*See Figure 1.*) During 2012, there were significantly fewer customer-found bugs compared with 2011.

2. **Actual results exceeded expectations based on the predicted model for Vivado customer-found bugs.** (*See Figure 2.*) The predicted model includes factors such as the number of new lines of code introduced (10 million) and the number of users (early adopters). Actual results were better than predictions by a significant margin and surpassed the Xilinx best-case model.

Figure 1. Customer-found CRs (high-priority only) for 2011 and 2012 (CY) – all families and applications

Figure 2. Model vs. actual customer-found bugs for Vivado (aligned by quarter after introduction)

3. **Customer-found bugs for 7 series designs were lower compared with customer-found bugs for 6 series.** (*See Figure 3.*) Overall design tool quality was improved (6 series support was only in IDE; 7 series support was in both IDE and Vivado) in the latest generations.

Figure 3. Architecture-specific customer-found bugs, origin aligned by quarter

BUILDING BETTER CUSTOMER DESIGNS

Customer Success = Xilinx Success

Xilinx has a long legacy of delivering products and services that accelerate the customer design process. Customers have access to an infrastructure that is continuously tuned to target defect-free product experiences. While this initiative takes a tremendous level of focus and partnership, the rewards have been extraordinary.

Xilinx has proven repeatedly that structured customer collaborations with high-volume customer applications can achieve levels close to, or at, zero PPM. This disciplined approach creates synergy between Xilinx and customers through joint design reviews, design evaluation samples, and focused teamwork. These collaborative efforts often extend to provide contract manufacturers with customer engineering support. By working with Xilinx, designers can enjoy superior results through:

- *Defect avoidance through collaborative knowledge sharing (training and tutorials) and design reviews*
- *Better customer experiences with debug tools (including access to design evaluation samples)*
- *Improved customer design methodologies through the introduction of Vivado™ design rule checks (DRCs) and a new handbook focused on design methodologies*
- *Fewer RMAs through improved development tool quality*

Xilinx began conducting customer seminars and presentations to improve customer design methodologies during 2012 and will continue this effort into 2013. The main focus areas are disseminating key FPGA design methodologies based on common lessons learned from more than 10,000 customer interactions across the Xilinx customer base.

INDUSTRY-LEADING SOFT-ERROR TESTING AND MITIGATION

Since 2001, Xilinx has been an industry leader in development and testing of single-event upset (SEU) solutions. Today, SEU solutions are crucial for all safety-critical markets including communications, avionics, automotive, industrial, and medical.

Years of Xilinx engineering effort and innovation have resulted in extraordinary advances, trusted partnerships, and patented SEU solutions. Today, at 28nm, the 7 series and Zynq™-7000 families leverage solutions for lowest-ever soft-error rates for configuration memory as well as for high-speed user-block memory. Building on this foundation, Xilinx offers industry-leading tools and mitigation solutions including the Xilinx FIT Rate Calculator, Soft Error Mitigation (SEM) IP, Essential Bits Technology, and lockstep soft-processor solutions.
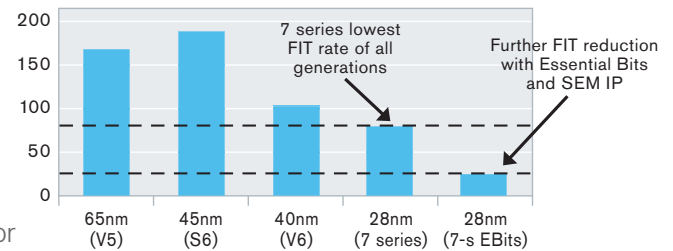

Figure 1. SEU Fit rate improvements between generations

Xilinx offers developers in-depth SEU knowledge, guidance, and solutions that provide the ability to detect, correct, and discriminate "care" vs. "don't care" upsets—all with minimized detection and recovery times. Target designs can now detect all upsets with certainty for naturally occurring soft-error events. Xilinx SEM IP allows for fault injection in any device configuration bit, which in turn gives the designer insight into device and system-level behavior, allowing for advanced assessment and mitigation testing.

CASE STUDIES

Demonstrated Xilinx Superiority

| SOLUTIONS	DEMONSTRATED TECHNOLOGY
Expertise	❯ Xilinx work led to JESD89A update
Heritage	❯ Since 2001, public / published data, improved silicon design, more IP, patents, and tools
Transparency	❯ Public disclosure of FIT / Mbit testing (lower at 28nm than ever before)
Predictability	❯ Published FIT Rate Calculator and tools for analysis of device / design FIT rate
Solutions	❯ Supported for detection, correction, classification, error injection, and beam results
Certainty	❯ User can detect if a design has been upset (not true for ASICs/CPUs)
Results	❯ Xilinx devices are immune to latch-up (unlike other FPGA manufacturers' products)

Figure 2. Demostrated technology expertise solutions

Essential Bits Technology allows the designer to unconditionally ignore more than 66% of upsets and designate a portion of the device as critical or not. Regardless of whether the upset matters, the SEM IP can repair 99.9% of all naturally occurring upsets, which is crucial for preventing an accumulation of errors in high-availability systems. The correction capability allows the user to avoid long recovery times associated with basic CRC checking, which requires reprogramming the full device to recover from soft errors. Detection and correction can be accomplished within tens of milliseconds.

For the most critical designs, Xilinx additionally offers lockstep soft-processor solutions that enable immediate detection of microprocessor faults. It is crucial for safety-critical systems designers to consider SEU detection, correction, and recovery, and Xilinx equips safety-critical designers with capabilities that are unmatched by any other semiconductor solution on the market.

Achieve >3x Increase in System Availability with Xilinx SEM IP and Essential Bits

Figure 3. User functional selection with prioritized essential Bits
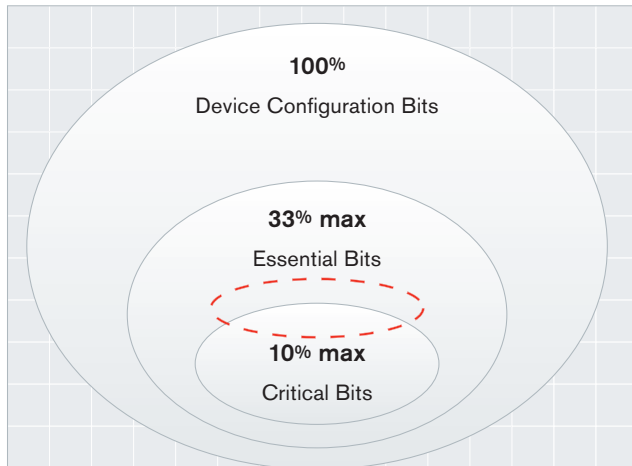
- *>66% reduction in system upset with essential bits*
- *Bits that cause functional upset are captured in essential bits*
- *User functional selection with prioritized essential bits, offering:*
  - *Increased fidelity in system handling of SEUs*
  - *Essential bits are masked for the specific function*
  - *All critical bits for that function are captured*

The Xilinx design tools include the Xilinx SEU FIT Rate Calculator. This tool takes into account altitude, longitude, latitude, solar activities, and device utilization to dynamically calculate estimated FIT rates for designs implemented in Virtex®-5, Virtex-6, Spartan®-6, and 7 series FPGAs prior to mitigation.

For More Information

Read the Xilinx white paper, "Considering Surrounding Single-Event Effects in FPGAs, ASICs, and Processors,"* for a broad overview of soft-error effects.

Please read about Xilinx reliability data in the UG116 Device Reliability Report. See the avionics developers' site** for more details about handling SEU effects in terrestrial and airborne applications. This page contains links to SEU mitigation design tools and the Xilinx SEU FIT Rate calculator.

  * http://www.xilinx.com/support/documentation/ white_papers/wp402_SEE_Considerations.pdf

** http://www.xilinx.com/applications/aerospace-and-defense/avionics/index.htm

Σ Guidance

Σ Solutions

Σ Knowledge

Σ Tools

Figure 4. Illustration of Xilinx's developer tools and documentations