INCREASING BANDWIDTH, SCALABILITY, AND INTEGRATION FOR REDUCED INFRASTRUCTURE CAPEX AND OPEX

ALL PROGRAMMABLE MULTI-MODE RADIO: MEETING MULTI-STANDARD, MULTI-BAND, MULTI-ANTENNA NEEDS WITH FEWER COMPONENTS

⟩ Challenges

- Meeting the demand for high transmission efficiency

- Designing flexible, low-cost multi-mode radio solutions that support multiple connectivity standards

- Accommodating low power and thermal efficiency constraints

- Scaling designs to support heterogeneous networks

- Driving down BOM costs and driving up reliability

⟩ Xilinx Radio Solution

- Highest level of integration, implementation for lower power and cost with higher reliability

- Xilinx CFR and DPD IP, providing more than 40% PA efficiency

- JESD204A/B, CPRI and OBSAI IP cores with serial transceivers to speed time to market

- Highly parameterizable IP to meet scalability and performance needs of heterogeneous networks

- Standardized interfacing for ease of integration

- Class-leading evaluation and development boards from Tektelic, Analog Devices, and Texas Instruments

The demand for increasing coverage and capacity is driving the rapid expansion in heterogeneous networks encompassing femtocells, picocells, microcells, macrocells, and active antenna systems. Furthermore, in addition to the increasing number of form factors, the complexity increases even further when also considering the increasing number of frequency bands, air interface standards, growth in signal bandwidth and the rise in multi-antenna MIMO systems. The Xilinx Radio portfolio—spanning All Programmable FPGAs and SoCs, IP building blocks, design tools, reference designs, and development boards—is ideally suited for meeting the current needs of high-throughput radio systems. As a result, Xilinx digital radio solutions are fully flexible and can scale to support multiple standards, wider bandwidths, and varying performance needs of heterogeneous networks while also drastically reducing development time, increasing system integration and flexibility to enable manufacturers to respond quickly to the demands of network providers.

CapEx and OpEx Reduction Through High Transmission Efficiency

Typical transmission efficiencies with 3G air interfaces on LDMOS* power amplifiers are in the range of 8 to 15%. Using advanced digital algorithms, efficiencies can be increased to 35 to 45% (50%+ with GaN**) with the latest-generation power amplifiers and Xilinx crest factor reduction (CFR) and digital pre-distortion (DPD) LogiCORE™ IP. This translates to significant savings per year in operational expenditure (OpEx). Capital expenditure (CapEx) is also reduced by enabling the use of smaller transistors in the power amplifiers, to deliver the same transmission power rating at the mast.
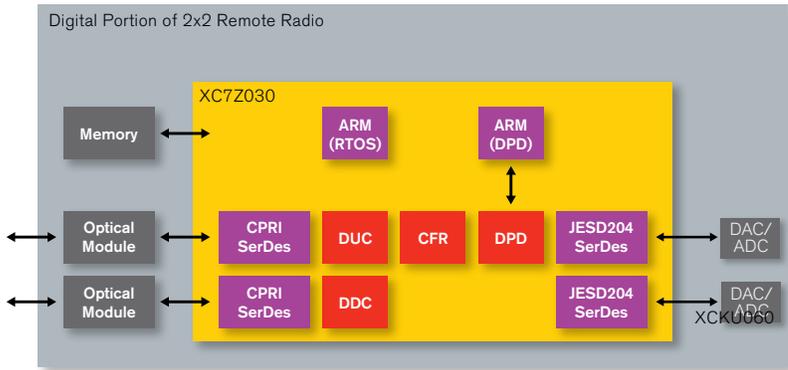
Integration Is Key to Low Power, Low Cost and High Reliability

Replacing multiple ASSPs with a single Xilinx All Programmable FPGA or SoC results in the smallest digital PCB footprint. Xilinx devices combine a rich mix of high-performance DSP and logic resources for efficient implementation of digital up conversion (DUC), digital down conversion (DDC), CFR, and DPD algorithms with multi-gigabit transceivers (MGTs) capable of implementing CPRI , OBSAI, or JESD 204A/B connections. Xilinx All Programmable SoCs' on-chip ARM processors and peripherals allow the further removal of external control processors for a single-chip radio implementation. Integrating all elements of radio processing in an All Programmable SoC allows the smallest, lightest, lowest-power and lowest-overall-cost radio equipment.

*Laterally Diffused Metal Oxide Semiconductor

**Gallium Nitride

⟩ XILINX

ALL PROGRAMMABLE™

ZYNQ-BASED DESIGN EXAMPLE FOR 2X20MHZ (40MHZ) 2X2 LTE RADIO

Digital Portion of 2x2 Remote Radio

XC7Z030

Memory

ARM (RTOS)   ARM (DPD)

Optical Module

CPRI SerDes   DUC   CFR   DPD   JESD204 SerDes   DAC/ADC

Optical Module

CPRI SerDes   DDC   JESD204 SerDes   DAC/ADC

XCKU060

RESOURCE REQUIREMENTS RUNNING 368MHZ

FUNCTION	SOURCE	LUT	DSP	RAM
2 Carrier 20MHz DUC (2Tx)	Xilinx	2,087	23	1
2 Carrier 20MHz DDC (2Rx)	Xilinx	2,498	30	1
3 Iteration CFR [6 6 6] (2Tx)	Xilinx	8,549	45	21
2Tx DPD power: on Zynq	Xilinx	7,026	35	47
CPRI Master and Slave	Xilinx	6,325	0	5
JESD 204B (2 Lane)	Xilinx	3,340	0	2
Total		22,130	133	77

28% LUTs, 33% DSP, 29% BRAM of Z-7030 with estimated total on-chip power: 8.521W.

ZYNQ-BASED DESIGN EXAMPLE FOR 5X20MHZ (100MHZ) 8X8 TD-LTE RADIO

Digital Portion of 8x8 Remote Radio

XC7Z100

Memory

ARM (RTOS)   ARM (DPD)   JESD204 SerDes   DAC/ADC

JESD204 SerDes   DAC/ADC

DUC   CFR   DPD   JESD204 SerDes   DAC/ADC

DDC   JESD204 SerDes   DAC/ADC

XC7Z100

ARM (RTOS)   ARM (DPD)   JESD204 SerDes   DAC/ADC

JESD204 SerDes   DAC/ADC

Optical Module

CPRI SerDes   DUC   CFR   DPD   JESD204 SerDes   DAC/ADC

Optical Module

CPRI SerDes   DDC   JESD204 SerDes   DAC/ADC
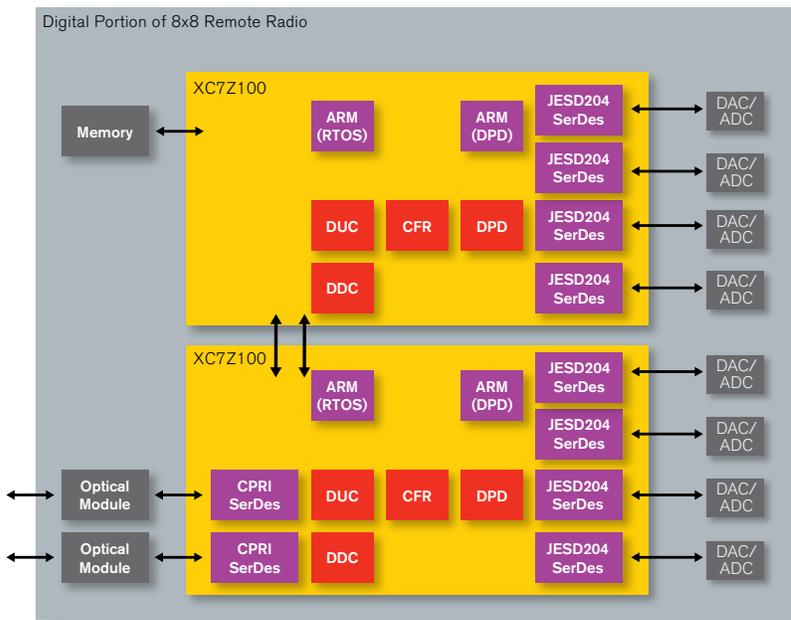
RESOURCE REQUIREMENTS RUNNING 245/368MHZ

FUNCTION	SOURCE	LUT	DSP	BRAM
5x20MHz (100M) DUC (4 Tx)	Xilinx	21,930	272	2
5x20MHz (100M) DDC (4 Rx)	Xilinx	32,485	280	0
4 Iteration CFR [6,6,4,4] (4 Tx)	Xilinx	35,691	80	212
4Tx DPD V7.0 HWA (1x)**	Xilinx	36,848	496	311
CPRI Master and Slave	Xilinx	4,280	0	8
JESD204B (4A 8 Lane)	Xilinx	4,512	0	4
Total		135,746	1,264	401

59% LUTs, 63% DSP, 53% BRAM of 7-Z100 with estimated on-chip power: 15.714W.

*DPD V7.0 EA is larger due to the need for Polyphase
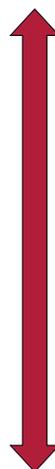
XILINX RADIO SOLUTIONS IP

PRODUCT	FAMILY SUPPORT	FEATURE HIGHLIGHTS
JESD204B	6 series 7 series Zynq-7000 AP SoC	▪ 1, 2, 3, 4, 5, 6, 7, or 8 lanes ▪ Scrambling and lane align ▪ Physical and data-link layers ▪ High-speed connection to MGTs at line rates up to 12.5Gbps
CPRI	6 series 7 series Zynq-7000 AP SoC	▪ Designed to CPRI V5.0 ▪ Supported line rates: 614Mbps to 10.1Gbps ▪ Auto-negotiation ▪ Master/Slave PHYs leveraging low-power MGTs ▪ 1 to 32 antenna-carriers per core
DUC/DDC Compiler	6 series 7 series Zynq-7000 AP SoC	▪ LTE (FD/TD-LTE), WCDMA or TD-SCDMA support ▪ 1-30 carriers per antenna ▪ 1-8 antennas ▪ Selectable IO sample rates
PC-CFR	6 series 7 series Zynq-7000 AP SoC	▪ LTE (FD/TD-LTE), CDMA2000, WCDMA, TD-SCDMA, WiMAX or MC-GSM (including frequency hopping) and multi-RAT ▪ Support for up to 100MHz BW in single-RAT and up to 80 MHZ in multi-RAT configurations ▪ 1-8 antennas ▪ Programmable latency ▪ 1-8 iterations ▪ Output peak to average power ratio (PAPR) of ~ 7dB at <4% error vector magnitude (EVM) ▪ >70dB adjacent channel leakage ratio (ACLR)
DPD	6 series 7 series Zynq-7000 AP SoC	▪ LTE (FD/TD-LTE), CDMA2000, WCDMA, TD-SCDMA, WiMAX or MC-GSM (including frequency hopping) and multi-RAT ▪ 1-8 antennas ▪ Optional QMC ▪ Optional hardware acceleration ▪ Up to 40dB ACLR correction ▪ Support for 100MHz+ BW ▪ 40%+ efficiencies in power amplifiers ▪ Selectable polynomial architecture support for area vs performance trade-off

- ▪ Seamless scalability, supporting typical antenna array combinations such as 2T2R, 2R4R, 4T4R, and 8T8R.
- ▪ Dedicated peripherals for memory controllers and connectivity using All Programmable SoC processing sub-system (PSS), such as DDR2/3, UARTS, Gigabit Ethernet, SPI, I2C etc.

HETEROGENEOUS NETWORK SOLUTION

Equipment	Configuration	Utilisation	Power
Femtocell	• 1Tx, 1Rx • 1x20MHz* LTE DUC/DDC	**Zynq-7010** 22% Logic, 45% DSP, 0% BRAM	307mW***
Picocell	• 1Tx, 1Rx • 1x20MHz* LTE DUC/DDC • CFR, DPD	**Zynq-7020** 28% Logic, 36% DSP, 25% BRAM	708mW***
Microcell	• 2Tx, 2Rx • 1x20MHz* LTE DUC/DDC • CFR, DPD	**Artix-7 7A100T** 39% Logic, 64% DSP, 43% BRAM	710mW**
		Kintex-7 7K70T 58% Logic, 48% DSP, 42% BRAM	1.036W**
		Zynq-7020 47% Logic, 70% DSP, 42% BRAM	1.082W***
Macrocell/ RRH	• 4Tx, 4Rx • 1x20MHz* LTE DUC/DDC • CFR, DPD****	**Kintex-7 7K160T** 55% Logic, 51% DSP, 48% BRAM	2.181W**
		Zynq-7030 65% Logic, 76% DSP, 59% BRAM	2.38W***
AAS	• 20MHz* LTE DUC/DDC implemented in central device	**Kintex-7 7K325T, Zynq-7030** Central Device	4.7W (K7)
	• CFR, DPD in distributed device	**Artix-7 7A100T (2x2), Kintex-7 7K160T (4x4)** Distributed Device	710mW (A7) 2.22W (K7)

* - 122MHz I/O sample rates ** - Core Dynamic, Static only *** - Core Dynamic, Static only + PSS
**** - DPD set to max performance (4x4 matrix), QMC on, 7th order Polynomials, All hardware accelerators
NOTE: Artix-7 clock = 245MHz clock; Kintex-7 clock = 368MHz

## Heterogeneous Network Solution Scalability

As OEMs develop solutions for heterogeneous networks, it is quickly disproved that 'one size fits all.' A choice of Xilinx devices and radio IP allows designers to smoothly scale from a low-complexity implementation such as a picocell to a high-end installation such as a wide-bandwidth multi-antenna macrocell. ASICs and ASSPs cannot match this scalability, and instead result in solutions that are limited to a fixed set of criteria and a narrow range of equipment. Xilinx All Programmable FPGAs and SoCs, combined with leading radio IP, allow customers to meet the needs of heterogeneous networks while maximizing cost efficiency, shortening time to market, and retaining full hardware and software flexibility.

Multi-Mode Radio Demonstration & Evaluation Platforms

Wireless radio subsystems must be designed with consideration for their environment. This is especially true of complex algorithms such as digital pre-distortion, where analog effects such as thermal and reactive transistor memory and analog signal chain behavior are not easily modelled. Xilinx has collaborated with the leading board vendors and data converter manufacturers to create a high-performance multi-mode radio demonstration platform showcasing DPD solutions with third-party power amplifiers at various frequencies and any air interface.

HIGH PERFORMANCE RADIO DEVELOPMENT BOARDS FEATURING TEKTELIC
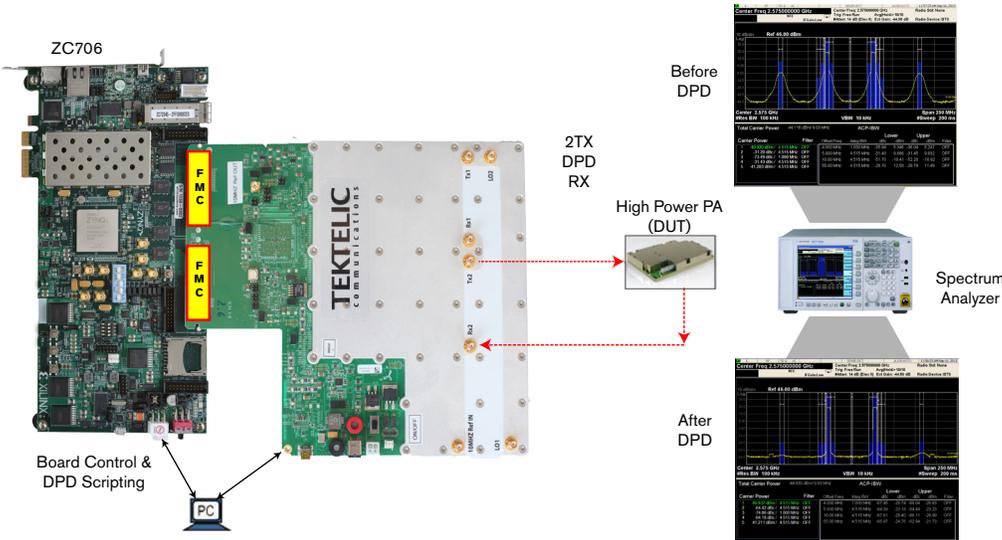
Features

Xilinx Zynq AP SoC ZC706 Board

- SFP connector supports connectivity requirements of OBSAI and CPRI
- Zynq AP SoC enables development of complex DUC /DDC, CFR, and DPD algorithms for any waveform
- For full specification, visit: http://www.xilinx.com/products/boards-and-kits/EK-Z7-ZC706-G.htm

Tektelic MSR Board

- Support for 100MH z+ transmission bandwidth
- Configurable at assembly for RF frequencies over 700MH z - 2.7GHz
- Meets stringent MC-GSM performance requirements
    - 2Tx, 2 DPD Rx (MIMO, Digital Doherty etc)
    - 170MHz Tx BW, High dynamic range (MC-GSM)

Example Performance Plots

- Freescale pallet: MD7I2020N driver + 2xMRF20165W final stage
- Test condition: TM3.1 LTE5 placed at edge of band
- Note: Tests carried out with Tektelic MSR board

SIGNALS	CONFIGURATION	POUT (dBm)	FINAL STAGE EFFICIENCY (%)	ACLR/IM3 (dBc)	SEM (dBm)
LTE20-FDD	[111], 60 MHz	45.1	43%	-54.55	-25.88
LTE5-FDD	[100..001], 65 MHz	49	40%	-58.2	-19.5

PERFORMANCE PLOTS
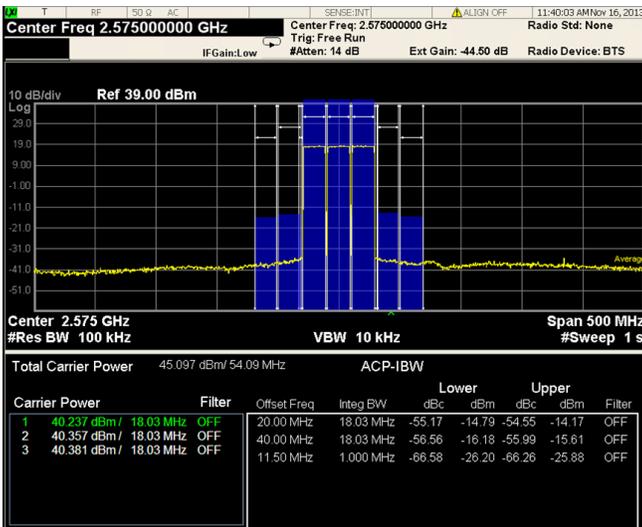
Plot 1: 3 LTE20-FDD carriers in 60MHz
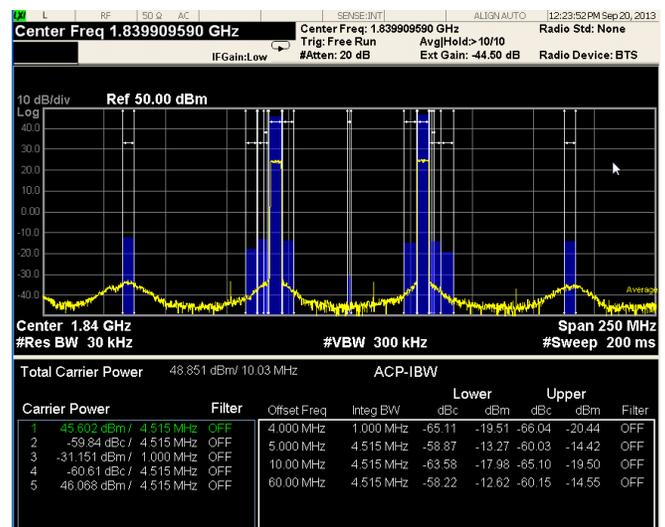
Plot 2: 2 LTE5-FDD carriers at band edges of 65MHz

For more information on the Tektelic board for Xilinx, please visit http://www.tektelic.com

UltraScale Architecture for Next-Generation High-Speed Wideband Radio Designs

Xilinx has introduced the next-generation UltraScale™ devices and Vivado® Design Suite to enable the development of next-generation, high-performance systems. The UltraScale devices deliver ASIC-class, system-level performance for the most demanding next-generation applications that requires massive logic resource, massive I/O and massive DSP and packet-processing performance at the highest level of utilization without degradation in performance. The growth driver for UltraScale in radio designs is for high-end wireless applications evolving to high-order MIMO architecture and to wideband operation with multiple bands and bandwidths. This means simultaneous use of non-contiguous channels in aggregate bandwidth of over 100MHz. This shift is driven by the next generation of LTE and LTE-Advanced, where peak rates are defined as over 1Gbps at low mobility.

The UltraScale architecture significantly reduces power consumption over 28nm devices, allowing high-order MIMO and wideband radios to be designed to meet thermal constraints (e.g. 100MHz 8x8 Radio). UltraScale devices can meet the corresponding connectivity needs by supporting 10.1Gbps CPRI line rate in addition to 12.5Gbps SERDES for JESD204. Furthermore, the UltraScale architecture has been designed in conjunction with the Vivado Design Suite to operate with high resource utilization (>80%) while operating at 491MHz system performance at the slowest speed grade. Although UltraScale architecture does not directly reduce cost over 28nm devices, the additional SERDES performance, power reduction, higher DSP density and high-speed operation means that UltraScale devices can offer total BOM cost reduction over multi-chip designs.

ULTRASCALE-BASED DESIGN EXAMPLE FOR 5X20MHZ (100MHZ) 8X8 TD-LTE RADIO

Digital Portion of 8x8 Remote Radio

RESOURCE REQUIREMENTS RUNNING 491MHZ
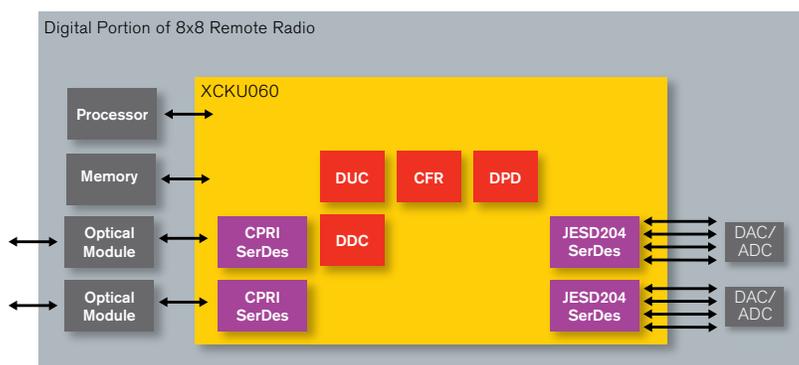
FUNCTION	SOURCE	LUT	DSP	BRAM
5x20MHz (100M) DUC (8 Tx)	Xilinx	43,860	544	4
5x20MHz (100M) DDC (8 Rx)	Xilinx	64,971	560	0
4 Iteration CFR [6,6,4,4] (8 Tx)	Xilinx	71,382	160	424
8 Tx DPD V7.0* HWA (1x)	Xilinx	75,311	1021	599
CPRI x4	Xilinx	8,560	0	16
JESD204B (8A 16 Lane)	Xilinx	9,024	8	0
Total		262,224	2,446	778

79% LUTs, 72% DSP, 88% BRAM of XKU060 with estimated total on-chip power: 21.523W

*DPD V7.0 estimates based on using Microblaze and Hardware Accelerators.

Take the NEXT STEP

For more information about Xilinx solutions for Radio, please visit http://www.xilinx.com/wireless

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe
Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan
Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.
Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

XILINX
ALL PROGRAMMABLE™