



FASTEST TIME TO MARKET,  
LOW TCO, FOR BEST-IN-CLASS  
100G PER-FLOW TRAFFIC MANAGER  
WITH FEATURE-RICH QOS

## ADDRESSING CRITICAL HIGH-BANDWIDTH NEXT-GENERATION NETWORK NEEDS TODAY

### » Xilinx Traffic Management Leadership

- The only FPGA-based traffic management solution capable of scaling between 20Gbps to 100Gbps and beyond
- Single FPGA implementation capable of up to 150 million packets per second (Mpps) throughput with 64-byte packets and minimal inter-packet gap (IPG)
- Ease of parameterization of link bandwidth, number of flows, levels of hierarchy, quality of service (QoS) controls, and more—all available on a single platform
- IP solution purposefully tuned for Xilinx FPGAs architecture and scalable across high-end enterprise, data center, and service provider networks
- Virtex®-6 HXT FPGA evaluation platform now in production, with industry-leading 6.6Gbps GTX transceivers and 11.18Gbps GTH transceivers
- Smooth migration roadmap from a legacy design or from Virtex-6 HXT FPGAs onto higher-bandwidth, lower-power, and better cost-to-power feature ratios of 28nm Xilinx Kintex™-7 and Virtex-7 FPGA families offering even wider array of transceiver and logic options

The non-stop introductions and growth in popularity of new laptops, notebooks, tablets, smart phones, and other web-connected devices continue to drive the demand for higher-bandwidth next-generation networks. Combined with the large number of concurrent applications—already synchronized across multiple web-connected devices—for each user, network complexity is also increasing exponentially, requiring higher numbers of flows that must be controlled individually through the enterprise, data centers, and service provider networks. Meanwhile, users are expecting and demanding maximum performance and better quality of experience from each of their applications.

Continuing its long history of innovation in wired communications, Xilinx currently delivers a highly integrated solution encompassing packet processing and traffic management. An array of connectivity IP cores, together with a reference design, provides the industry's first FPGA-based per-flow 100G traffic manager with feature-rich QoS controls. Applications based on Xilinx Virtex-6 FPGAs offer fine-grained parameterization, and are positioned to smoothly and rapidly transition to next-generation, lower-power, and lower-cost 28nm Xilinx 7 series devices that enable single-chip line cards and higher-bandwidth processing.

### The Power of Programmability for 100G Traffic Management

For decades, traffic management line cards were based on custom ASICs and NPUs. Each configuration would typically address a specific networking segment. Traditionally, these silicon solutions tried to keep up with the evolving industry by either overbuilding silicon to address upcoming requirements with multiple sets of features, or by adding post-deployment software upgrade services. Both alternatives increased the total cost of ownership. With disparate networking elements rapidly converging into all-IP networks and many standards being realigned, the service providers and system operators saw a need for “hitless” in-system upgrades. As a result, OEM vendors have increasingly turned to programmable logic to build more affordable systems that can flexibly scale, support field upgrades, and be customized to specific market needs.

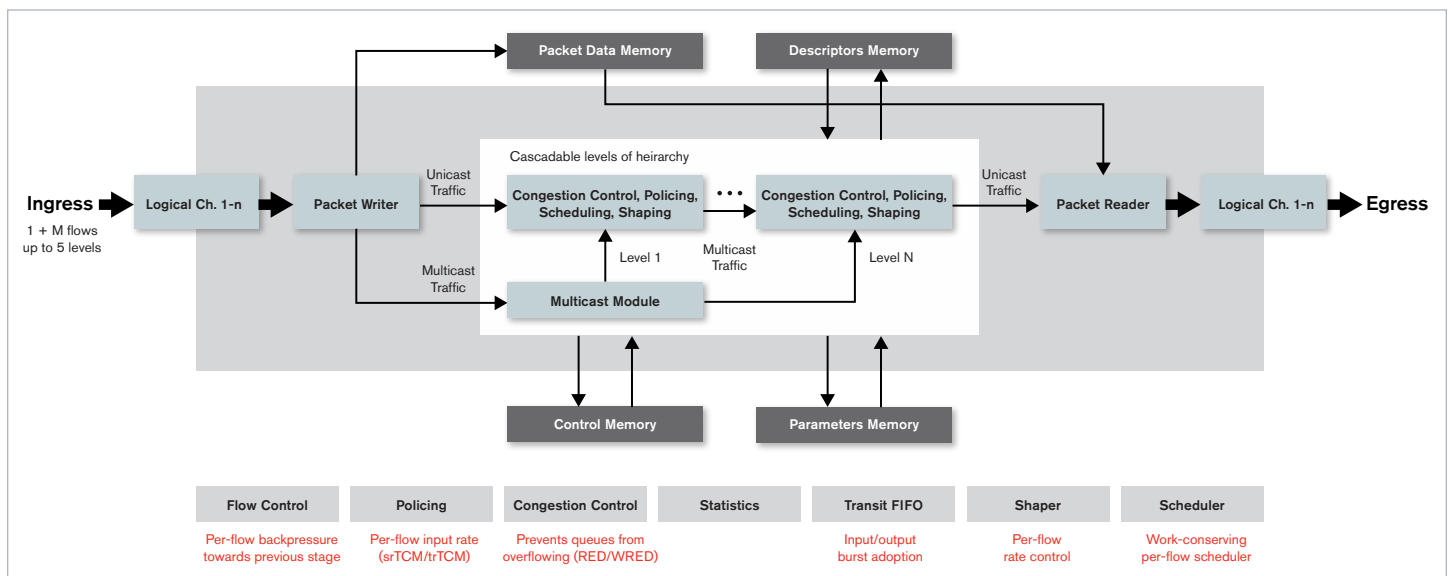
Xilinx FPGAs alleviate frequent hardware upgrade cycles, and enable next-generation, highly scalable, easily parameterized traffic management solutions tailored for high-bandwidth networks. Xilinx devices make it possible to build in fine-grained QoS capabilities for meeting the most complex service-level agreements (SLAs) across networking markets from service provider, enterprise, and data center segments. The Xilinx technologies and design methodologies are enabling ecosystem friendly designs, with groundbreaking reductions in power consumption, advanced heat transfer, and ultimately improved yields. The versatility and efficiency of the programmable, in-socket upgradeable Xilinx devices eliminate field replacements, time-consuming software regression tests, and costly field-validation cycles.

## Hierarchical Per-Flow Traffic Manager Functionality

Based on a common, unified architecture, Xilinx FPGAs enable next-generation traffic management and packet-processing applications with a broad feature set. Highlights include, but are not limited to:

- Up to five levels of hierarchical scheduling
- More than 1M queues, with easy aggregation to any level of the hierarchy
- Superior traffic burst equalization
- Random Early Detection (RED) and Weighted RED (WRED), with per-queue drop thresholds
- Policer logic, with per-flow, dual-token bucket supporting the Two Rate Three Color Marker (trTCM) algorithm described in IEEE RFC 2698
- Per-flow scheduling logic, through Strict Priority (SP), Round Robin (RR), Weighted Round Robin (WRR), Weighted Fair Queuing (WFQ), or Deficit Weighted Round Robin (DWRR) methods
- Per-flow shaper logic, with token bucket shaping
- Per-queue statistics
- Multiple backpressure mechanisms at any level of hierarchy
- Support for unicast, multicast, and broadcast traffic
- Throughput of up to 150 million packets per second with 64-byte packet and minimum inter-packet gap (IPG)
- Support for jumbo frames

## TRAFFIC MANAGER



## Advanced IP Ecosystem

The Xilinx ecosystem gives designers a portfolio of optimized Xilinx and third-party IP and hardware reference designs that speed integration and market adoption. The peripheral and traffic management blocks (and providers) that leverage the unified architecture of the 6 and 7 series include:

- 10GE MAC, 100GE MAC, and Interlaken controller
- QDR2+ controller
- DDR2/3 controller
- UART
- TCAM/KPB interface
- Packet classifier.
- Hierarchical per-flow traffic manager

## Examples of Applications

- Single-Channel 100GE Traffic Manager line card for enterprise routers (single-chip Virtex-6)
- Dual-Channel 100GE Traffic Manager line card for enterprise routers (single-chip Virtex-7)
- Wireless Backhaul Packet Processing/Traffic Manager line card
- Edge QAM line card
- High-Bandwidth xPON line card

## Getting Started

Today, customers can build 100G traffic management systems based on the in-production Virtex-6 HXT FPGAs, which offer 6.6Gbps GTX and 11.18Gbps GTH transceivers for industry-leading serial bandwidth.

The Xilinx packet processing reference platform based on Virtex-6 FPGAs allows system architects to evaluate a first-in-class 100G traffic management IP use case that offers:

- Throughput of up to 150 million packets per second with 64-byte packet and minimum inter-packet gap (IPG)
- Up to three levels of hierarchical scheduling
- Up to 8K queues, with easy aggregation to any level of the hierarchy
- Weighted RED (WRED) with per-queue drop thresholds
- Per-flow policer with dual-token bucket supporting the Two Rate Three Color Marker (trTCM) algorithm per IEEE RFC 2698.
- Per-flow scheduling logic, through Strict Priority (SP and Deficit Weighted Round Robin (DWRR).
- Per-flow shaper logic, with token bucket shaping.
- Per-queue statistics
- Multiple backpressure mechanisms at any level of hierarchy
- Support for unicast, multicast, and broadcast traffic
- Support for jumbo frames

To discuss other use cases, please contact a Xilinx sales representative.

## Migration to 28nm FPGAs

Xilinx 6 series and 7 series FPGAs have in common a unified architecture. As solutions architects evolve requirements for high bandwidth systems—by increasing ports numbers, levels of hierarchies, numbers of flows, and per-flow policing, marking, and shaping controls—the Xilinx unified architecture enables rapid migration to next-generation 28nm 7 series FPGA families. Kintex™-7 and Virtex-7 FPGAs support a wide array of memory controllers and high memory bandwidth to address the most demanding packet processing and traffic management configurations. With the highest port density of any FPGA in its class, the Kintex-7 FPGA family supports up to 32 12.5Gbps transceivers. The Virtex-7 HT FPGA family offers up to 72 13.1Gbps transceivers or up to 16 28Gbps transceivers.

## Xilinx: Driving Innovation

Xilinx developers continue to drive innovations into the intelligent data processing plane. Coupled with the traffic management solution, the IP solutions under development include 100G packet parsing and payload manipulation solutions, carrier Ethernet services, low-latency switching, and many others. Please talk to your local sales representative if you have a specific requirement related to packet processing applications.

Xilinx labs are also involved in research to push beyond the current bandwidth boundaries. One innovation currently being developed is a 400 Gbps packet processing engine with a specialized packet parsing language offering protocol-agnostic language. This research shows promise not only for yielding very compact resource-efficient FPGA block instantiation but is also addressing a new intelligent data path programming approach.

## For More Information

To learn more about Xilinx traffic management device features and application development methodologies, as well as the kits, reference designs, and platforms that can accelerate design projects, visit [www.xilinx.com](http://www.xilinx.com) or call your local sales office to schedule a discussion with a Xilinx traffic management application specialist.

### Corporate Headquarters

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
USA  
Tel: 408-559-7778  
[www.xilinx.com](http://www.xilinx.com)

### Europe

Xilinx Europe  
One Logic Drive  
Citywest Business Campus  
Saggart, County Dublin  
Ireland  
Tel: +353-1-464-0311  
[www.xilinx.com](http://www.xilinx.com)

### Japan

Xilinx K.K.  
Art Village Osaki Central Tower 4F  
1-2-2 Osaki, Shinagawa-ku  
Tokyo 141-0032 Japan  
Tel: +81-3-6744-7777  
[japan.xilinx.com](http://japan.xilinx.com)

### Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific  
5 Changi Business Park  
Singapore 486040  
Tel: +65-6407-3000  
[www.xilinx.com](http://www.xilinx.com)

