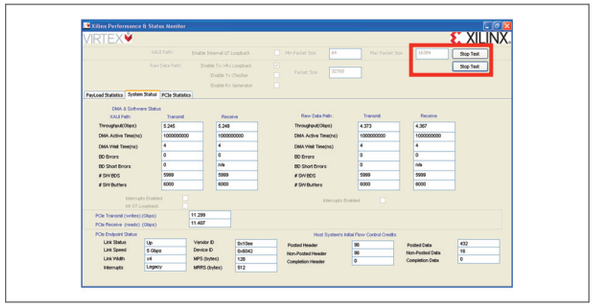
STEP 9

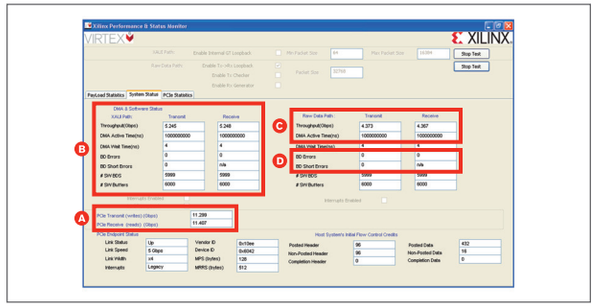


Performance Monitor Application: Start Data Traffic

A. Click on Start Test to begin XAUI data transfer.

B. Click on Start Test to begin Raw data transfer.

STEP 10



Performance Monitor Application: Verify Data Throughput and Error Free Operation

A. Confirm PCIe Throughput.

B. Confirm DMA Channel throughput for the XAUI path.

C. Confirm DMA Channel throughput for the Raw Data path.

D. Confirm Error Free operation - no Buffer Descriptor Errors.

Congratulations! The Virtex-6 FPGA Connectivity Kit is now set up. The pre-built connectivity targeted reference design demonstration has been tested, using the built-in block for PCI Express (x4 PCI Express Gen2 Endpoint), XAUI LogiCORE IP, a Virtual FIFO memory controller designed to interface to the on-board DDR3 memory, and Northwest Logic's high performance DMA controller for PCI Express.

Next, please refer the Getting Started Guide included in this kit. The guide provides further instructions on running the demo, evaluating and modifying the design files – Hardware RTL design and Software Device Driver. For updated information on this Virtex-6 FPGA Connectivity Kit, please visit **www.xilinx.com/v6connkit.**

Support Information

To download Design Tools, generate license or get the latest tool updates go to www.xilinx.com/support/download.

For Technical Support, go to www.xilinx.com/support. On this site you can:

- Subscribe to Alerts on Product Technical Documentation updates
- Choose instructor-led classes and recorded e-learning options under Training
- Collaborate with the Xilinx User Community on the Forums
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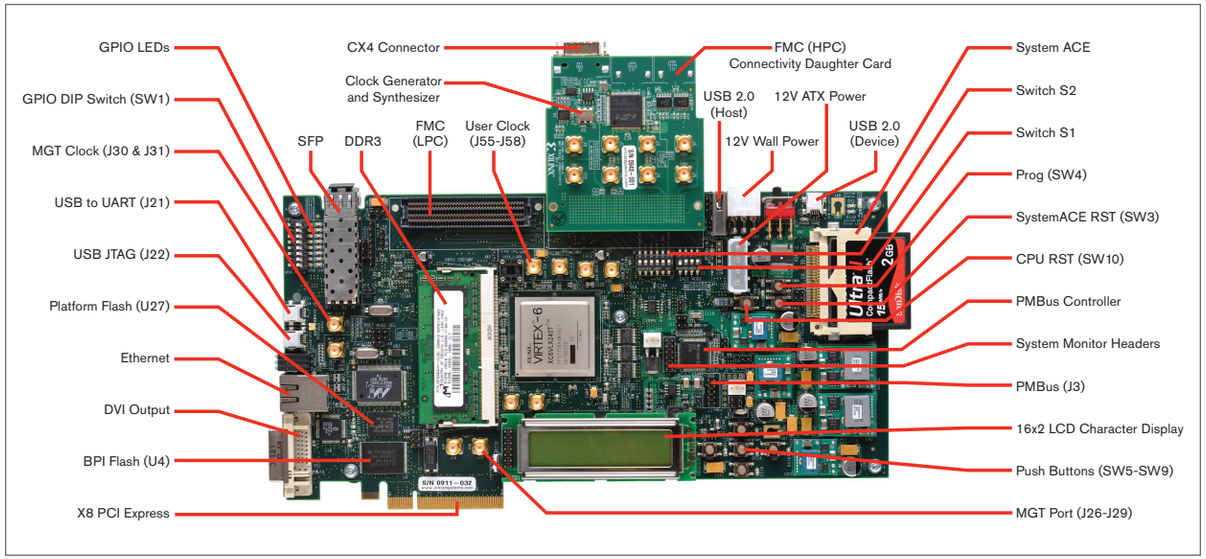
HARDWARE SETUP GUIDE VIRTEX-6 FPGA CONNECTIVITY KIT

FOR MORE INFORMATION GO TO WWW.XILINX.COM/V6CONNKIT

VIRTEX-6 FPGA CONNECTIVITY KIT HARDWARE SETUP GUIDE

This Hardware Setup Guide provides step-by-step instructions to setup the ML605 board, the FMC daughter card, and run the pre-built Demo that uses the built-in block for PCI Express (x4Gen2 configuration), XAUI IP LogiCORE, a Virtual FIFO Memory controller interfacing to the on-board DDR3 memory and a third-party PCIe DMA Controller.

BOARD FEATURES



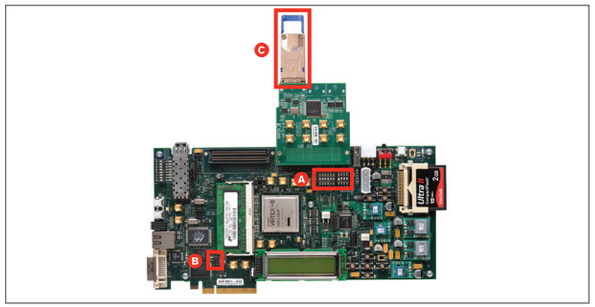
Kit Contents

- ML605 board and FMC Connectivity Daughter Card
- CX4 Loopback Connector
- Universal 12V power supply
- 2 USB A / Mini-B cables
- 1 ethernet Cat5 cable
- 1 DVI-to-VGA adapter
- 4 SMA cables
- 1 SATA cable, 1 SATA loopback cable
- 1 CompactFlash card (2GB)
- Xilinx ISE Design Suite DVDs
- 1 USB stick
- Windows driver and GUI
- Documents include a welcome letter, Hardware Setup Guide, Getting Started Guide

What's Needed for Demonstration

- Xilinx Virtex-6 FPGA Connectivity Kit
- Windows XP 32 bit PC system with a x8/x16 PCIe slot on the motherboard and a USB port
- Keyboard & Mouse
- Monitor

STEP 1



Board Setup and Configuration

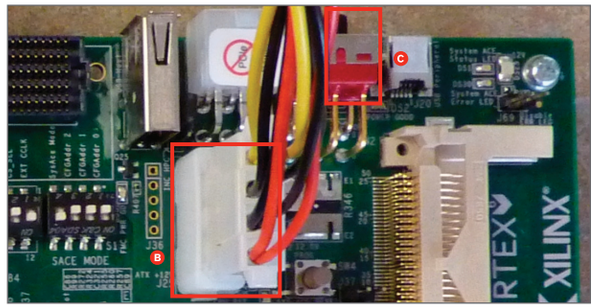
The ML605 is shipped with the FMC Connectivity Daughter Card module attached to the FMC_HPC connector. To run the demonstration, you will need to externally loopback the XAUI data using a CX4 loopback connector provided in the kit.

A. Ensure correct Switch Settings:
- S1: 1-OFF, 2-OFF, 3-OFF, 4-ON
- S2: 1-ON, 2-OFF, 3-OFF, 4-ON, 5-ON, 6-OFF

B. Ensure Jumper J42 block: pins3-4 are shorted

C. Plug in the CX4 loopback connector:
- Plug the CX4 loopback connector on the FMC Connectivity Daughter card's J2 connector.

STEP 2



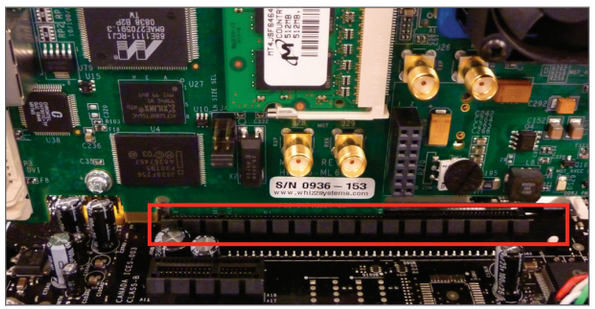
Connect the Power Connector

A. Turn the PC system OFF.

B. Connect the PC systems' 12V ATX power supply's available 4-pin disk drive-type power connector to the board (J25).
Warning: Using any other power supply connector other than the 4-pin in-line connector, will result in damage to the PC system and the ML605 board.

C. The power switch SW2 should be switched to the ON position (away from the bracket edge).

STEP 3



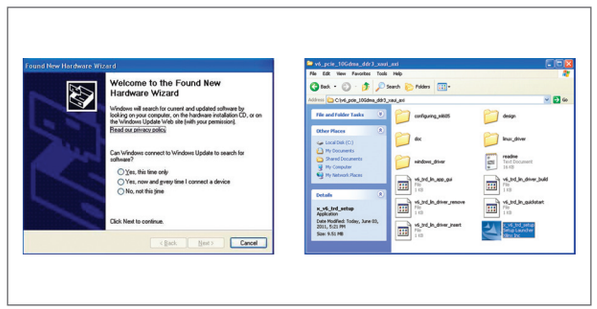
Insert ML605 Board into PCIe Express Slot

A. Identify the x8 / x16 PCIe Express slot on the PC motherboard.

B. Insert the ML605 board into the PCI Express slot through the PCIe x8 edge connector.

C. Turn the power ON. The PCIe 10GDMA DDR3 XAUI targeted reference design will be loaded from the Platform Flash.

STEP 4



With ML605 installed, Boot the PC

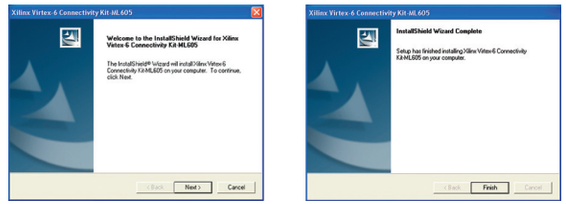
A. Cancel New Hardware Found Window.

B. Mount the USB FLSASH drive and copy the V6_pcie_10Gdma_ddr3_xaui_axi folder to the PC system.

C. Run x_v6_trd_setup.exe to install GUI, copy drivers and find HW.

For further information, please refer to the Virtex-6 FPGA Connectivity Kit Getting Started Guide for more details.

STEP 5



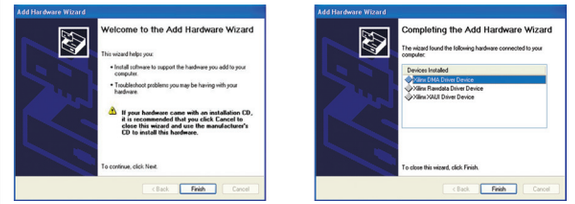
First Installer Window | Last Installer Window

Continue to Copy Files and Install GUI

A. Click Next 3 times to continue install process (select typical).

B. When InstallShield Wizard Complete screen is displayed click on Finish.

STEP 6



First Driver Window | Last Driver Window

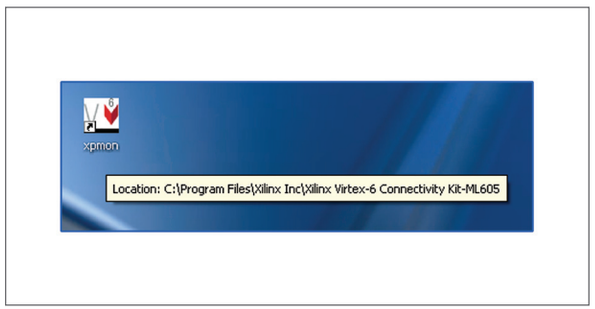
Load XDMA, RawData and XAUI Device Drivers

A. The PCI Simple Communications Controller VID:10EE DID:6042 will attach to the XDMA driver.

B. Two child drivers RawData and XAUI will install and attach to the XDMA driver.

C. Select "No not this time" , "Install the software automatically" and Next for each of the 3 drivers.

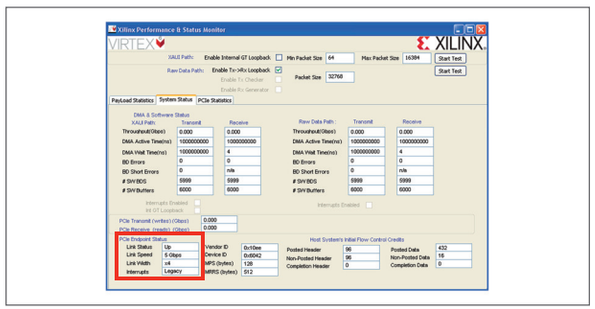
STEP 7



Launch Xilinx Performance Monitor Application

A. Click the xpmon icon on the desktop to launch the Xilinx Performance Monitor Application GUI.

STEP 8



Performance Monitor Application: Verify Board Status

Click on the **System Status** tab to confirm board status and PCIe settings:

A. Link Status: Up

B. Link Speed: 5.0Gbps

C. Link Width: x4