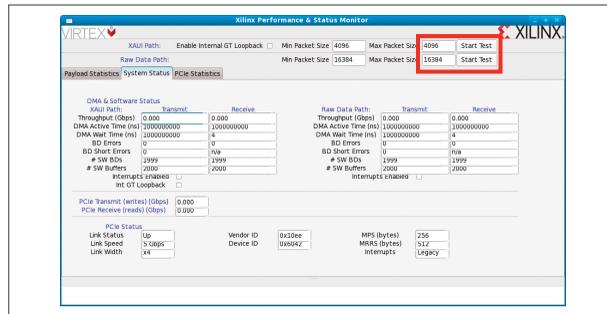


STEP 9



Performance Monitor Application: Start Data Traffic

- A. Click on Start Test to begin XAUI data transfer.
- B. Click on Start Test to begin Raw data transfer.

Congratulations! The Virtex-6 FPGA Connectivity Kit is now set up. The pre-built connectivity targeted reference design demonstration has been tested, using the built-in block for PCI Express (x4 PCI Express Gen2 Endpoint), XAUI LogiCORE IP, a Virtual FIFO memory controller designed to interface to the on-board DDR3 memory, and Northwest Logic's high performance DMA controller for PCI Express.

Next, please refer the Getting Started Guide included in this kit. The guide provides further instructions on running the demo, evaluating and modifying the design files – Hardware RTL design and Software Device Driver. For updated information on this Virtex-6 FPGA Connectivity Kit, please visit [www.xilinx.com/v6connkit](http://www.xilinx.com/v6connkit).

Support Information

To download Design Tools, generate license or get the latest tool updates go to [www.xilinx.com/support/download](http://www.xilinx.com/support/download).

For Technical Support, go to [www.xilinx.com/support](http://www.xilinx.com/support). On this site you can:

- Subscribe to Alerts on Product Technical Documentation updates
- Choose instructor-led classes and recorded e-learning options under Training
- Collaborate with the Xilinx User Community on the Forums
- Quickly scan titles of Answers Database categories through the Answer Browser
- Submit cases and report bugs online 24 hours a day through WebCase
- Initiate and manage return of hardware and software products through the RMA Portal

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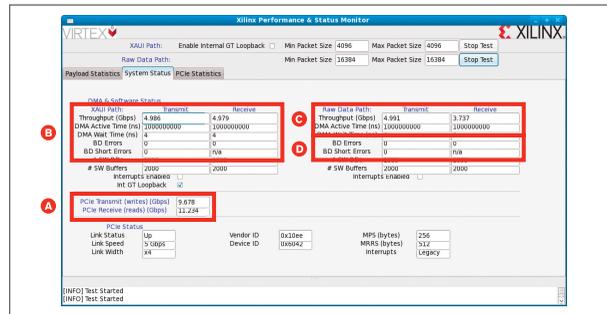
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STEP 10



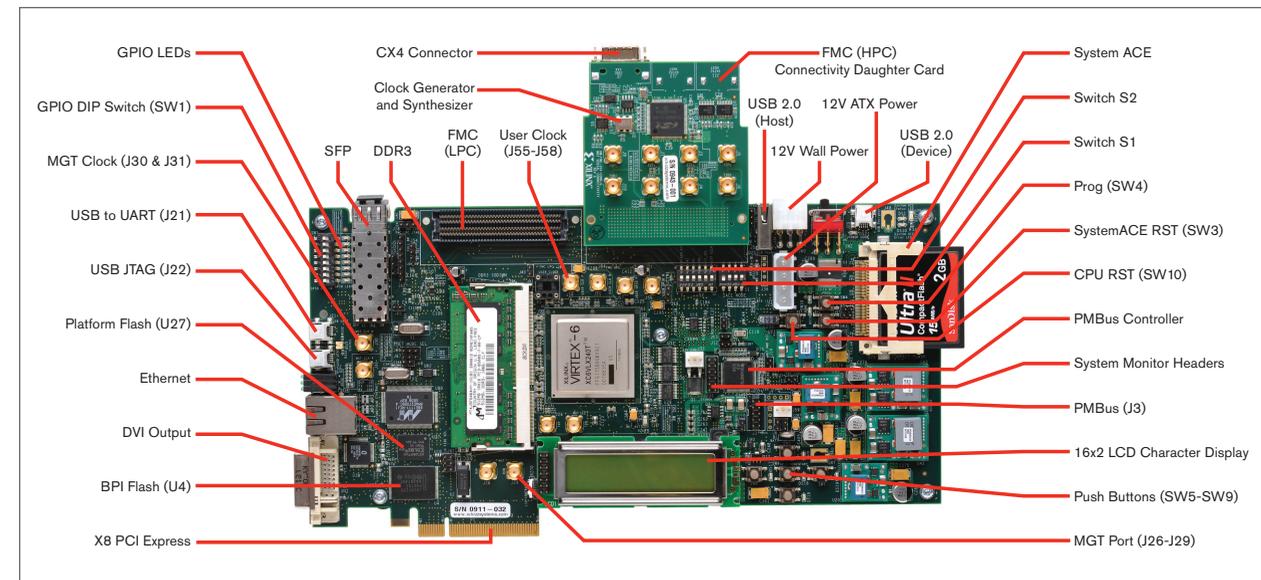
Performance Monitor Application: Verify Data Throughput and Error Free Operation

- A. Confirm PCIe Throughput.
- B. Confirm DMA Channel throughput for the XAUI path.
- C. Confirm DMA Channel throughput for the Raw Data path.
- D. Confirm Error Free operation - no Buffer Descriptor Errors.

VIRTEX-6 FPGA CONNECTIVITY KIT HARDWARE SETUP GUIDE

This Hardware Setup Guide provides step-by-step instructions to setup the ML605 board, the FMC daughter card, and run the pre-built Demo that uses the built-in block for PCI Express (x4Gen2 configuration), XAUI IP LogiCORE, a Virtual FIFO Memory controller interfacing to the on-board DDR3 memory and a third-party PCIe DMA Controller.

BOARD FEATURES



Kit Contents

- ML605 board and FMC Connectivity Daughter Card
- CX4 Loopback Connector
- Universal 12V power supply
- 2 USB A / Mini-B cables
- 1 ethernet Cat5 cable
- 1 DVI-to-VGA adapter
- Four SMA cables
- 1 SATA cable, 1 SATA loopback cable
- 1 CompactFlash card (2GB)
- Xilinx ISE Design Suite DVDs - 11.1 and 11.4 Update
- 1 USB stick
- Fedora Core 10 Live CD
- Documents include a welcome letter, Hardware Setup Guide, Getting Started Guide

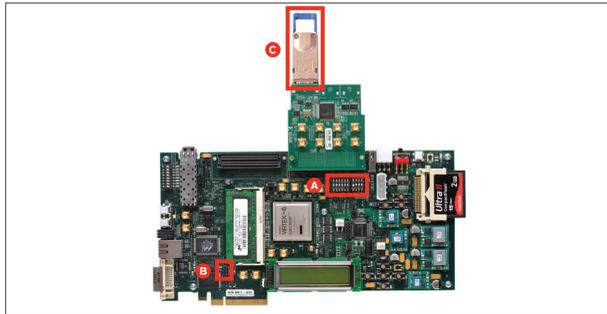
What's Needed for Demonstration

- Xilinx Virtex-6 FPGA Connectivity Kit
- PC system with a x8/x16 PCIe slot on the motherboard, CDROM drive and a USB port
- Keyboard & Mouse
- Monitor



FOR MORE INFORMATION GO TO  
[WWW.XILINX.COM/V6CONNKIT](http://WWW.XILINX.COM/V6CONNKIT)

STEP 1

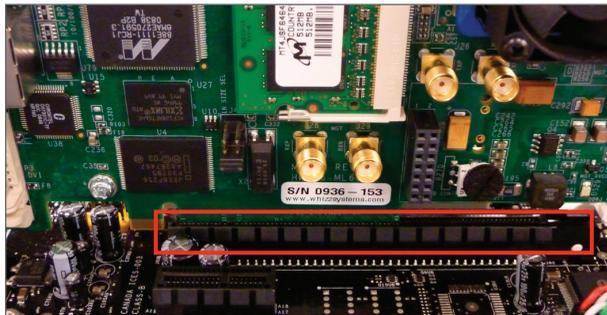


Board Setup and Configuration

The ML605 is shipped with the FMC Connectivity Daughter Card module attached to the FMC\_HPC connector. To run the demonstration, you will need to externally loopback the XAUI data using a CX4 loopback connector provided in the kit.

- A. Ensure correct Switch Settings:
  - S1: 1-OFF, 2-OFF, 3-OFF, 4-ON
  - S2: 1-ON, 2-OFF, 3-OFF, 4-ON, 5-ON, 6-OFF
- B. Ensure Jumper J42 block: pins3-4 are shorted
- C. Plug in the CX4 loopback connector:
  - Plug the CX4 loopback connector on the FMC Connectivity Daughter card's J2 connector.

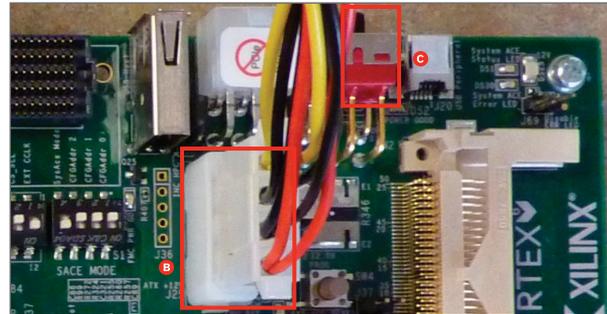
STEP 3



Insert ML605 Board into PCIe Express Slot

- A. Identify the x8 / x16 PCIe Express slot on the PC motherboard.
- B. Insert the ML605 board into the PCI Express slot through the PCIe x8 edge connector.
- C. Turn the power ON. The PCIe 10GDMA DDR3 XAUI targeted reference design will be loaded from the Platform Flash.

STEP 2



Connect the Power Connector

- A. Turn the PC system OFF.
- B. Connect the PC systems' 12V ATX power supply's available 4-pin disk drive-type power connector to the board (J25).
  - Warning: Using any other power supply connector other than the 4-pin in-line connector, will result in damage to the PC system and the ML605 board.
- C. The power switch SW2 should be switched to the ON position (away from the bracket edge).

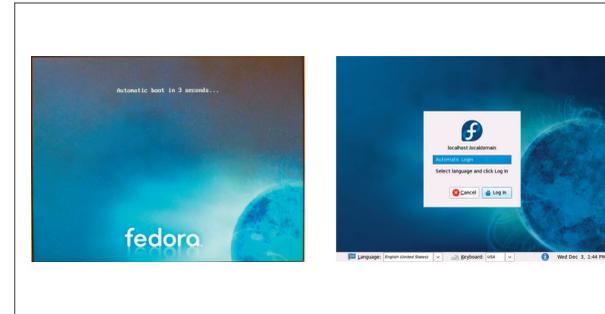
STEP 4

Boot PC from CD-ROM

- A. Configure the PC system to boot from the CD-ROM drive.
- B. Place the Fedora 10 Live CD into the CD-ROM drive.

For further information, please refer to the Virtex-6 FPGA Connectivity Kit Getting Started Guide for more details.

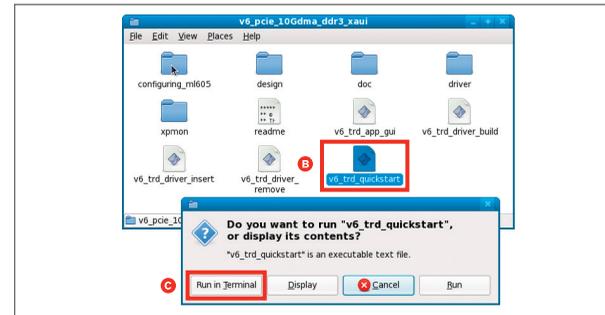
STEP 5



Boot Fedora 10 Live and Automatically Login

- A. The screens above will appear on Power UP.
- B. Wait two to three minutes depending on the system configuration for the PC to boot completely.

STEP 7



Load Driver and Launch Performance Monitor application

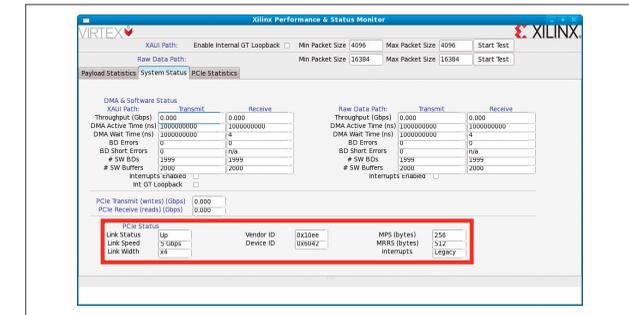
- A. Navigate to the v6\_pcie\_10Gdma\_ddr3\_xaui folder.
- B. Double-click v6\_trd\_quick\_start. This will build kernel objects, insert driver modules and launch the Performance Monitor Application GUI.
- C. Click Run in Terminal to proceed.

STEP 6

Copy Contents of USB Flash Drive

- A. The reference design files are provided on the USB flash drive delivered with the kit.
- B. Insert the USB flash drive into a USB connector of the PC system.
- C. Wait for the Fedora 10 OS to mount the USB flash. When the flash is mounted, an icon pops up on the desktop.
- D. Double-click on the USB flash drive icon and copy the v6\_pcie\_10Gdma\_ddr3\_xaui folder into the live user's home folder/directory.
- E. To unmount the USB flash, right-click on the USB flash drive icon and select Unmount Volume.

STEP 8



Performance Monitor Application: Verify Board Status

- Click on the System Status tab to confirm board status and PCIe settings:
- A. Link Status: Up
  - B. Link Speed: 5.0Gbps
  - C. Link Width: x4