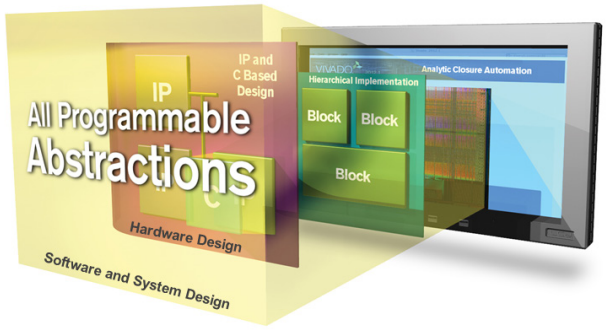
9 REASONS WHY THE VIVADO DESIGN SUITE ACCELERATES DESIGN PRODUCTIVITY

Does your development team need to create complex, competitive, next-generation systems in a hurry? Xilinx All Programmable devices take your team far beyond the bounds of conventional programmable logic and I/O by adding software-programmable ARM® processing systems, programmable Analog Mixed Signal (AMS) subsystems, and an expanding range of complex intellectual-property (IP) cores to the mix. You can also choose All Programmable devices based on various combinations of silicon die interconnected with high-performance, 3D, stacked silicon interconnect technology that's uniquely Xilinx. These generation-ahead All Programmable devices take you far beyond the abilities of conventional programmable logic to an era of fully programmable systems integration.

ALL PROGRAMMABLE ABSTRACTION AND AUTOMATION



What does that mean?

It means your team can incorporate more system functions into fewer parts, increase system performance, reduce system power consumption, and lower BOM cost with Xilinx All Programmable Devices while meeting tough time-to-market requirements. However, you cannot realize these benefits without powerful hardware, software, and system-design tools and design flows that put these benefits into the hands of your design team. Collectively, Xilinx calls the required hardware-, software-, and system-design flows "All Programmable Abstractions."

The backbone for advanced, generation-ahead hardware, software, and system development using All Programmable Abstractions is the Xilinx Vivado® Design Suite. The Vivado Design Suite delivers a comprehensive, SoC-strength, IP- and system-centric, generation-ahead development environment built from the ground up to address all of the productivity bottlenecks you commonly experience during system-level integration and implementation.

While competing solutions attempt to extend outdated and loosely connected point tools in an attempt to keep pace with the explosive growth in on-chip integration, the Vivado Design Suite provides a unique, highly integrated development environment that delivers radically improved design productivity with the industry's most advanced, SoC-strength design methodologies and algorithms. The Vivado Design Suite raises the productivity bar for hardware, software, and systems engineers alike.

Here are 9 reasons why the Vivado Design Suite can deliver generation-ahead design productivity, ease-of-use, and system-level integration:

Accelerate System Implementation

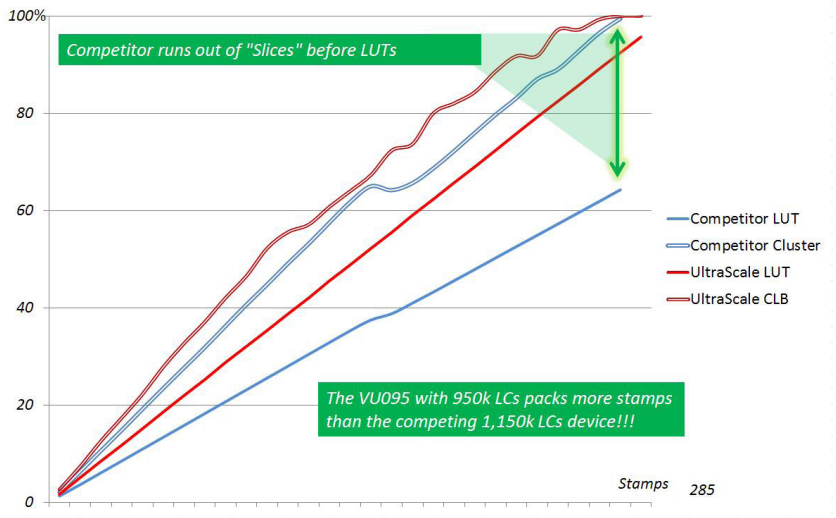
Reason 1: Push the device-density envelope: Fit more into a device, faster

A design tool's ability to fit more functions into an All Programmable device directly translates into system-level cost and power savings by allowing you to select the smallest possible device for your system design. The Vivado Design Suite maximizes the realized potential of an All Programmable device's programmable logic fabric and its dedicated, on-chip functional blocks by providing an integrated way for architecture, software, and hardware developers to work synergistically within a common design environment, which yields maximally efficient results.

For example, consider an Ethernet MAC (Media Access Controller) block design from OpenCores.org. As an experiment, Xilinx repeatedly stamped copies of an OpenCores Ethernet MAC until they filled a Virtex® UltraScale VU095 FPGA with 940,800 LCs (logic cells). Similarly, Xilinx filled a competing device that has 1,150,000 LCs. The following graph shows the results of this experiment.

Measured by logic cell count (a "standard" logic cell equals one 4-input LUT (Look Up Table) plus a flip-flop), the Virtex UltraScale VU095 has theoretically 18% less capacity than the competing device (with 1,150,000 LCs) but, as illustrated in Figure 1, the Xilinx Virtex UltraScale VU095 device accommodates 4% more instances of the Ethernet MAC block when the Vivado Design Suite fits all of these instances into the device. This experiment shows that the Vivado Design Suite combined with the Xilinx UltraScale architecture is far more efficient than the competing tool/device combination.

FIGURE 1: FABRIC RESOURCE UTILIZATION VERSUS NUMBER OF STAMPS



(Note: Figure 1 uses LUT and slice count results to compare the Xilinx UltraScale All Programmable device with a competing programmable-logic device. A Xilinx UltraScale All Programmable device slice consists of four 6-input LUTs, eight flip-flops, and associated multiplexers and arithmetic carry logic and is equal to 1.6 LCs.)

How the Vivado Design Suite maximizes device utilization

The Vivado Design Suite achieves high device utilization because it employs advanced fitting algorithms and because the Xilinx UltraScale architecture features truly independent LUTs within each slice. Note that the Xilinx UltraScale architecture fitting results for both LUTs and slices in the above graph track very closely and both achieve nearly 100% utilization while the competing programmable-logic device runs out of available slices after reaching only 64% device utilization. This lower utilization is a result of the competing device's programmable-logic architecture, which prevents in many situations the packing of two LUTs into a single physical cluster. In a full design, this clearly results in numerous underutilized clusters with only one LUT used while the second one becomes unusable for the rest of the design's logic due to pin sharing requirements imposed by the architecture. This experiment strongly suggests that you can use smaller Xilinx UltraScale All Programmable to realize larger system designs.

In stark contrast to the competitive results for this experiment in IP block fitting, the Vivado Design Suite achieves 99% LUT utilization and it can place and route this design while meeting timing constraints even with this high utilization level. The Vivado place-and-route algorithms are designed to handle dense, challenging designs, allowing you to put more logic into the device. That lowers your system BOM cost and reduces system power consumption.

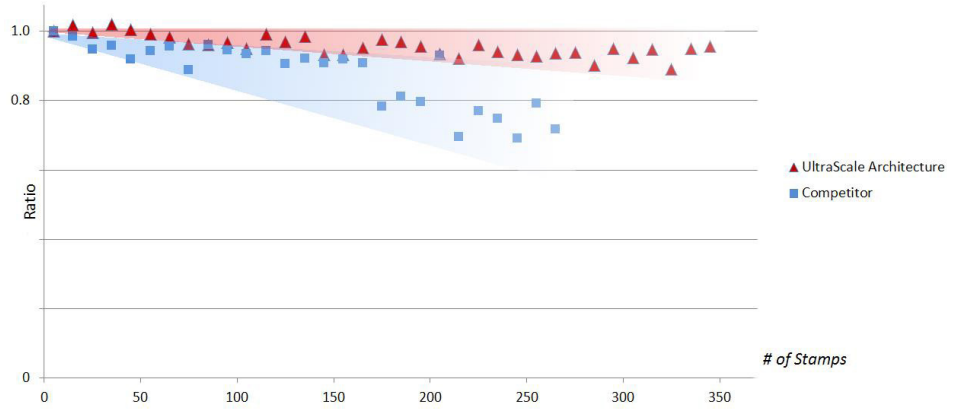
Reason 2: Vivado delivers robust performance and low power with predictable results

Due to the physics of nanometer IC design, interconnect has become the performance bottleneck in programmable-logic device architectures at 28nm and below. The Vivado Design Suite employs leading-edge place-and-route algorithms that break this performance bottleneck and can deliver high-performance results with push-button ease.

The Vivado Design Suite's analytical place-and-route algorithms deliver predictable design closure by concurrently optimizing across multiple variables including timing, interconnect usage, and wire length. Meanwhile, the Vivado implementation engine ensures that the results for large devices with high logic utilization are equally as good for designs with lower device utilization. In addition, the Vivado Design Suite maintains its high-performance results while providing more consistent results from one run to the next as the system design grows incrementally larger due to the addition of system features.

As figure 2 demonstrates, the Vivado Design Suite continues to deliver better performance results than the competition as utilization rises and handles larger designs as well.

FIGURE 2: NORMALIZED PERFORMANCE ACROSS NUMBER OF STAMPS



Note that Figure 2 shows that the competitor's results have an average variation that is four times larger than the results delivered by the Vivado Design Suite. Also note that the competing solution gives up as much as one third of the available performance as the device fills up. In stark contrast, the Vivado Design Suite delivers consistent results and maintains performance across the tested design variations. Finally, you should note that the competing solution cannot handle systems as large as those successfully handled by the Vivado Design Suite. The competing solution simply gives up sooner.

The benefits: the ability to handle larger system designs with better predictability and easier timing closure.

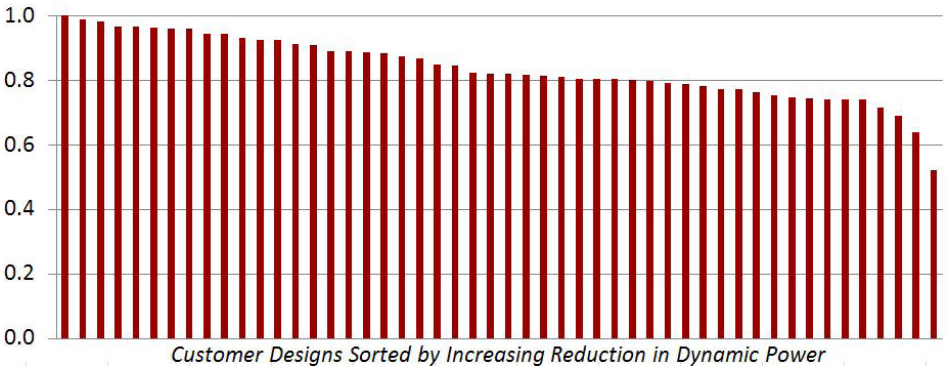
Vivado lowers system power

The Vivado Design Suite provides best-in-class tools for system power analysis and optimization. Starting at the architectural or device-selection stage, designers can rely on the accuracy and unparalleled ease-of-use of the Xilinx Power Estimator spreadsheet (XPE) to determine system power consumption. Easy design entry through the XPE's Quick Estimate and IP wizards and the ability to make simple side-by-side comparisons of multiple implementations give your design team the ability to fine tune settings to accurately model various scenarios.

As your design moves to the compilation stage, the Vivado Design Suite continues to offer accurate power analysis and estimation. Out of the box, the Vivado Design Suite provides automatic power reduction without adversely affecting your system design's timing. If you require additional power savings, you can employ the Vivado Design Suite's unique ability to leverage the Xilinx 7 series' fine-grained clock-gating technology to further reduce power consumption across an entire system design or just portions of it.

The intelligent clock gating optimizations made possible by the Vivado Design Suite can lower dynamic power by 18% on average, as illustrated by Figure 3.

FIGURE 3: DYNAMIC POWER RATIO WITH INTELLIGENT CLOCK GATING OPTIMIZATIONS (SORTED BY INCREASING GAIN)



An unmatched array of features helps you to easily analyze your design. You can identify the modules that consume the most power, thus pinpointing where to get the most benefit from your efforts to reduce system power consumption. All of these capabilities are built into the versatile Vivado Integrated Design Environment (IDE) so that your design team can minimize system power in one place, using just one unified suite of tools.

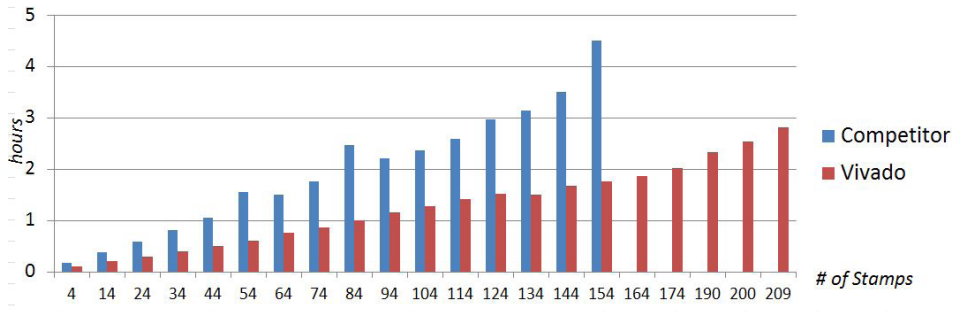
System power consumption is a significant factor in designing most products and the Vivado Design Suite provides generation-ahead design tools that complement Xilinx's All Programmable devices.

Reason 3: Vivado Design Suite delivers unparalleled runtime and memory utilization

Designer productivity requires design tools that run fast—preferably fast enough to permit multiple compilations per day so that the design team can quickly converge on a final design. The Vivado Design Suite was designed from the start to run quickly—much faster than competing programmable-logic design tools.

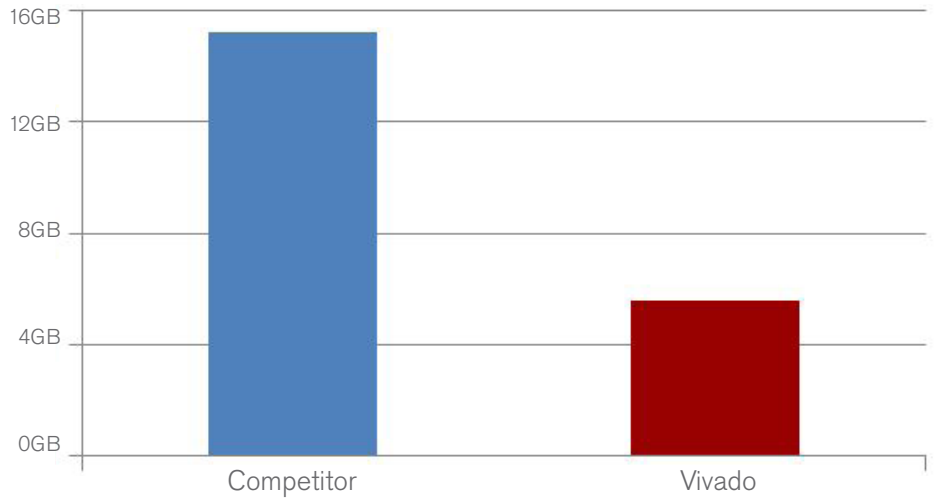
Consider the OpenCores Ethernet MAC block design example discussed above. Figure 4 shows that the Vivado Design Suite run time is as much as three times faster than the competitor's software as the number of instances grows. Additionally the data shows that the Vivado run time scales in a predictable way; the run time scales monotonically with design size. In stark contrast, run-time results for the competing software show anomalies. For example, a 94-instance design completes faster than a design using 84 instances.

FIGURE 4: RUNTIME COMPARISON



Vivado requires less memory

FIGURE 5: MEMORY USAGE



The Vivado Design Suite employs advanced, efficient data models and structures to yield the smallest memory footprint—substantially smaller than the memory footprint required by competing solutions. Continuing to use the OpenCores Ethernet MAC block example, the competing software required almost 16GB of RAM for its largest successful run (154 instances) while the Vivado Design Suite needed two thirds less RAM for a design of the same size, as shown in Figure 5. A reduced memory footprint translates into a significant productivity advantage for the Vivado Design Suite because designers can compile larger system designs without running out of memory.

Accelerate System Integration

Reason 4: C-based IP Generation with Vivado High-Level Synthesis

Today, wireless, medical, defense, and consumer applications are more sophisticated than ever and use more complex algorithms than ever before. The industry's gold standards for algorithm development are the C, C++, and SystemC high-level programming languages. Previously, there was a slow, error-prone step in the design process required to convert algorithms written in C, C++, or SystemC into Verilog or VHDL hardware descriptions suitable for synthesis. Vivado High Level Synthesis—part of the Vivado Design Suite System Edition—easily automates this process.

You may have heard of C-level hardware synthesis before. Whatever you may have heard, C-level algorithmic synthesis is now on the fast track for system-level design. More than 400 active users are successfully using Vivado High-Level Synthesis (HLS) to create hardware IP for Xilinx All Programmable devices from C, C++, and SystemC specifications.

Vivado HLS puts system and design architects on the fast track to hardware-IP creation through:

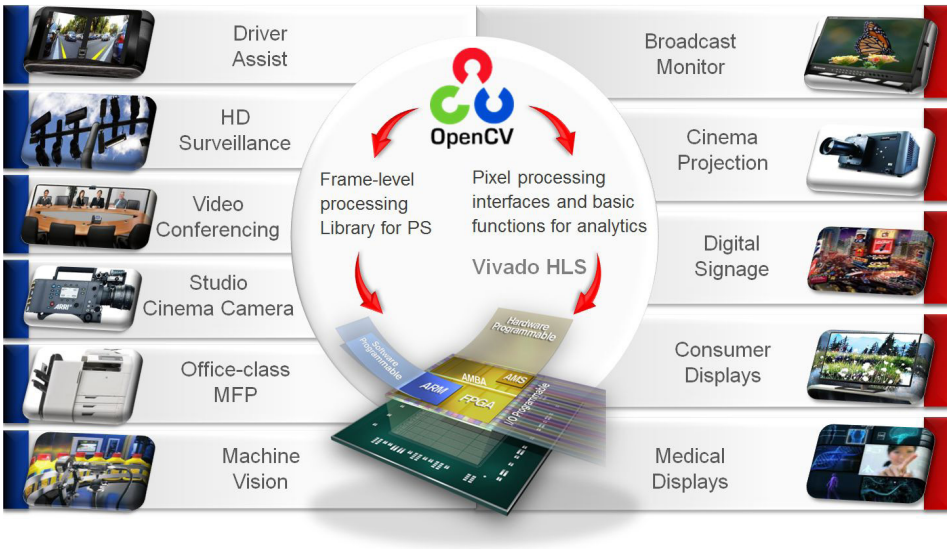
- Abstraction of algorithmic descriptions, data-type specifications (integer, fixed-point, or floating-point), and interfaces (FIFO, AXI4, AXI4-Lite, AXI4-Stream)
- A directives-driven, architecture-aware compiler that delivers the best possible QoR (Quality of Results)
- Accelerated block-level verification using C/C++ test bench simulation, automatic VHDL or Verilog simulation, and test bench generation
- Generated hardware IP that slips easily into the RTL-based design flow using the full Vivado Design Suite, model-based design using the Vivado System Generator for DSP, and block-based design using the Vivado IP Integrator

As a result, hardware designers have more time for design-space exploration, which means they have time to evaluate alternative architectures to find truly optimal design solutions to tough system-design challenges. For example, designers can accelerate complex linear algebra algorithm execution speeds by an order of magnitude (10X) while achieving better QoR than hand-coded RTL using Vivado HLS with industry-standard, floating-point math.h operations, as shown in Table 1.

TABLE 1: VIVADO HLS QOR

Radar Design (1024x64 floating-point QRD)	RTL Approach (VHDL)	Vivado Hls
Design Time (weeks)	12	1
Latency (ms)	37	21
Resources:		1
▪ BRAMS	273	38
▪ FFs	29,686	14,263
▪ LUTs	28,512	24,257

FIGURE 6: VIVADO HLS ACCELERATES OPENCV-BASED DEVELOPMENT



Vivado HLS also accelerates the development of real-time Smarter Vision algorithms for systems based on Xilinx Zynq®-7000 All Programmable SoC devices through pre-written, pre-verified vision and video functions integrated into an OpenCV® environment and they can run these algorithms using software on the Zync SoC's dual-core ARM® processing system and hardware on the Zynq SoC's high-performance FPGA fabric, as shown in Figure 6.

The Vivado HLS Smarter Vision library functions allow you to rapidly achieve real-time execution of complex pixel-processing interfaces and basic video analytics functions using hardware acceleration.

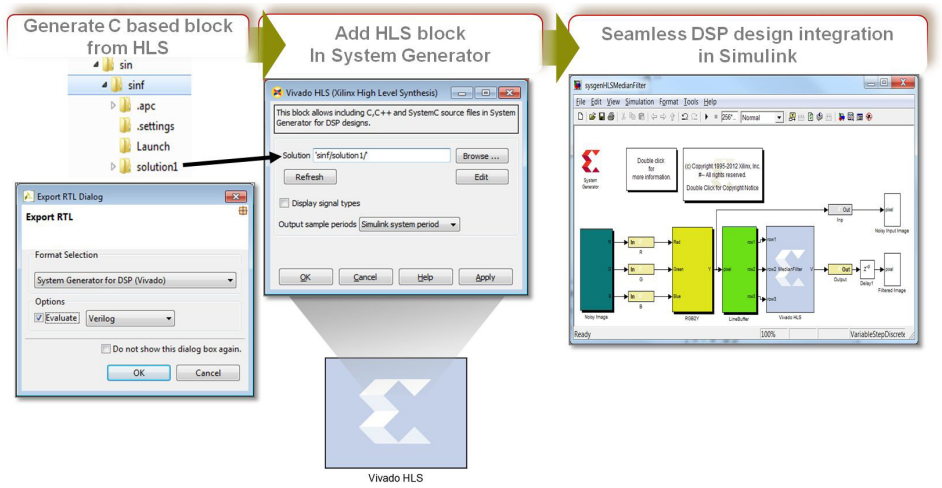
(Want to get started with Vivado HLS immediately? Download the **Introduction to FPGA Design with Vivado High-Level Synthesis**—a comprehensive User Guide based on training that Xilinx has successfully deployed with its top customers. This guide quickly teaches software engineers how to quickly accelerate their code by migrating software algorithms from processors to the programmable logic in Xilinx All Programmable FPGAs and SoCs.)

Reason 5: Model-based DSP design integration using System Generator for DSP

As mentioned above, the Vivado Design Suite System Edition includes System Generator for DSP, the industry's leading high-level design tool for converting DSP algorithms into high-performance, production-quality hardware in a fraction of time needed when using traditional RTL design methods. The Vivado System Generator for DSP accelerates the development of highly parallel systems by allowing developers to seamlessly integrate arithmetic functions, SmartCORE™ and LogiCORE™ IP, custom RTL, and C-based blocks synthesized into hardware with Vivado HLS using the industry's most advanced All Programmable system-modeling tools: Simulink™ and MATLAB™ from the MathWorks®. A design flow for integrating C-based blocks into Simulink using Vivado HLS and Vivado System Generator for DSP appears in Figure 7.

The Vivado System Generator for DSP further accelerates system implementation by providing automatic fixed-point or floating-point hardware generation, hardware co-simulation that accelerates Simulink simulation by as much as 1000X, system integration for use in the RTL-based Vivado design flow, and block-based design through the Vivado IP Integrator.

FIGURE 7: INTEGRATE C-BASED BLOCKS INTO SIMULINK USING VIVADO HLS AND VIVADO SYSTEM GENERATOR FOR DSP



Reason 6: Block-based IP integration with Vivado IP Integrator

The Vivado Design Suite shatters the RTL design-productivity barrier by providing the industry's first plug-and-play IP integration design environment: the Vivado IP Integrator.

Vivado IP Integrator provides a graphical and Tcl-based, correct-by-construction design flow. It offers a device- and platform-aware interactive environment with a powerful, integrated debug capability that supports intelligent auto-connection of key IP interfaces, one-click IP subsystem generation, real-time design-rule checks (DRCs), and interface change propagation.

Using Vivado IP Integrator, designers work at the "interface" and not the "signal" level of abstraction when making connections among IP blocks. This increased level of interface abstraction greatly increases designer productivity. Although the emphasis is on using industry standard AXI4 interfaces, IP Integrator also supports dozens of other commonly used interfaces.

By working at the interface level, design teams can rapidly assemble complex systems that leverage IP created with Vivado HLS, Vivado System Generator for DSP, Xilinx SmartCORE and LogiCORE IP, Alliance Member IP, and proprietary IP. The combination of Vivado IP Integrator and Vivado HLS can significantly reduce development costs—by as much as a factor of 15—versus an RTL approach.

FIGURE 8: ZYNQ DESIGN WITH HLS AND SYSTEM GENERATOR ACCELERATORS

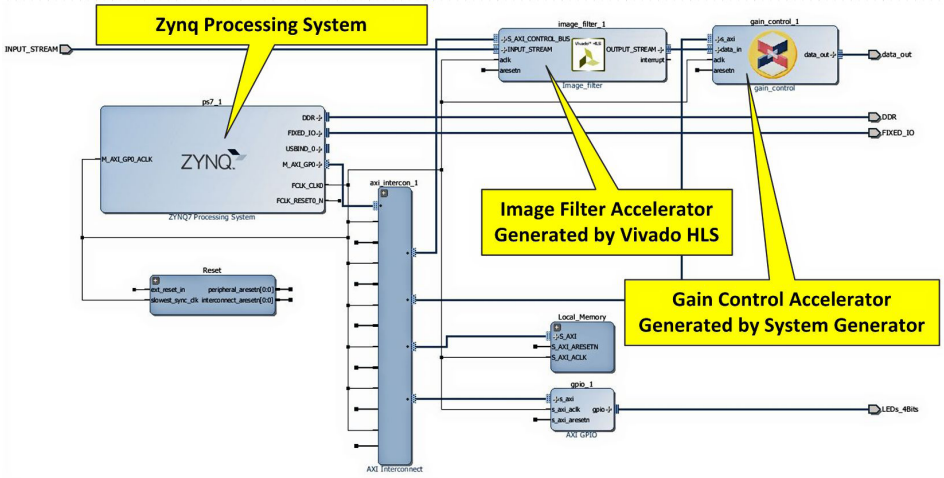


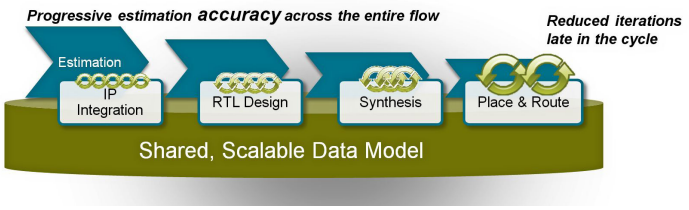
Figure 8 shows a Vivado IP Integrator view of a system-level design based on the Xilinx Zynq-7000 Processing System, an image-filter accelerator generated by Vivado HLS, and a gain-control accelerator generated by Vivado System Generator for DSP.

Accelerate System Verification

Reason 7: Vivado Integrated Design Environment for Design and Simulation

The Vivado Design Suite also provides a complete, fully integrated set of tools for design entry, timing analysis, hardware debug, and simulation encapsulated by a state-of-the-art IDE. The design-analysis feature of the Vivado Design Suite's IDE employs a shared, scalable data model to accommodate the extremely large All Programmable devices. The Vivado Design Suite employs this single data model throughout the design flows, providing the design team with continuous visibility into key design metrics including timing, power, resource utilization, and routing congestion much earlier and throughout the design process. Estimates become progressively more accurate as the design progresses, driving faster design closure with fewer design iterations.

FIGURE 9: THE VIVADO DESIGN SUITE MAINTAINS A SHARED, SCALABLE DATA MODEL THROUGHOUT THE DESIGN FLOW



The Vivado Design Suite is the only design solution that offers a mixed-language simulator as part of its integrated design environment. With competitive simulators, you must choose either VHDL or Verilog simulation. A mixed-language simulator is critical for the latest system designs that incorporate IP from many sources.

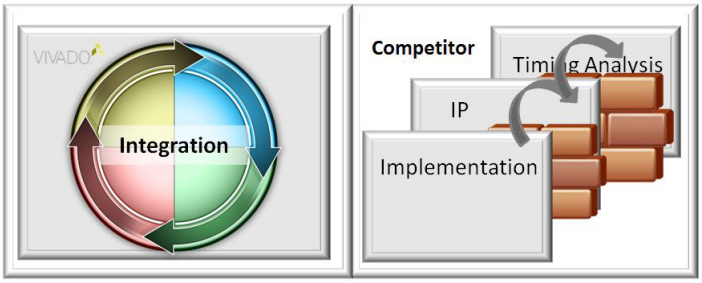
The Vivado Design Suite also uses a shared waveform viewer for simulation and debug that eliminates the learning curve when switching from a simulation environment to a hardware-debug environment. Competitive offerings force users two learn and use different tools with different waveforms to achieve these same tasks. Design teams work faster and avoid mistakes when simulation and debugging capabilities are fully integrated, as they are in the Vivado Design Suite.

Similarly, the cross-probing capabilities of competitive development tools are fragmented and extremely limited. Further, these cross-probing capabilities are usually restricted to one individual tool. In stark contrast, the Vivado Design Suite provides complete, integrated, front-to-back cross probing through all of the different design views: implemented design, synthesized design, timing reports, and all the way back to the design team's original RTL code.

The Vivado Design Suite's single-data-model architecture enables extensive cross-probing between design sources, schematic views, hierarchy browsers, design reports, messages, floorplan, and the Vivado Device Editor. This unique capability enables faster debug and timing closure by providing immediate design feedback about any design issues discovered during the entire system-development process.

In addition, competitive design solutions employ multiple disk files for inter-tool communications. The complexities and the inefficiencies resulting from the use of multiple disk files degrades tool performance and leads to multiple interfaces, greatly increasing the likelihood that tools will not communicate well among themselves. There is no such risk with the Vivado Design Suite, which employs a single shared data model for handling all aspects of the design, as shown in Figure 10.

FIGURE 10: THE VIVADO DESIGN SUITE'S SINGLE, SHARED DATA MODEL SMOOTHLY INTEGRATES ALL DESIGN ACTIVITIES



Reason 8: Comprehensive hardware debug

The Vivado Design Suite's probing methodologies are intuitive, flexible, and iterative. Designers can choose a probing strategy that best suits their design flow:

- RTL design files, synthesized design, and XDC constraint files
- Netlist insertion
- Interactive Tcl or scripts to automate probing

Advanced trigger and capture capabilities

The Vivado Design Suite provides advanced trigger and capture capabilities for detecting complex events. All trigger parameters are accessible during a debug session and you can examine or dynamically modify parameters on the fly without the need to recompile your design.

Zynq SoC cross triggering between Processor System (PS) and Programmable Logic (PL)

The Vivado Design Suite also supports cross triggering between the Processor System (PS) and the Programmable Logic (PL) in Zynq-7000 All Programmable SoC devices. This feature provides a means to co-debug an embedded design distributed across the Zynq PS and PL using the Xilinx Software Development Kit (SDK), Vivado IP Integrator, and the Vivado Logic Analyzer. Coupled with a powerful software debugger—the GNU Debugger (GDB) utility—the Vivado IP Integrator and Vivado Logic Analyzer allow designers to debug their software and hardware algorithms simultaneously. Designated interface signals are provided between the Zynq-7000 All Programmable SoC platform and the Xilinx ILA (integrated logic analyzer) IP core for seamless co-debugging operations.

Enabling hardware read and write in real-time – JTAG to AXI Master

The Vivado Design Suite can perform real-time read and write transactions between the Zynq PS and PL during hardware debugging. A new debug IP (JTAG to AXI Master) coupled with the easy-to-use IP Integrator flow enables access to data within any AXI-based IP block in a design.

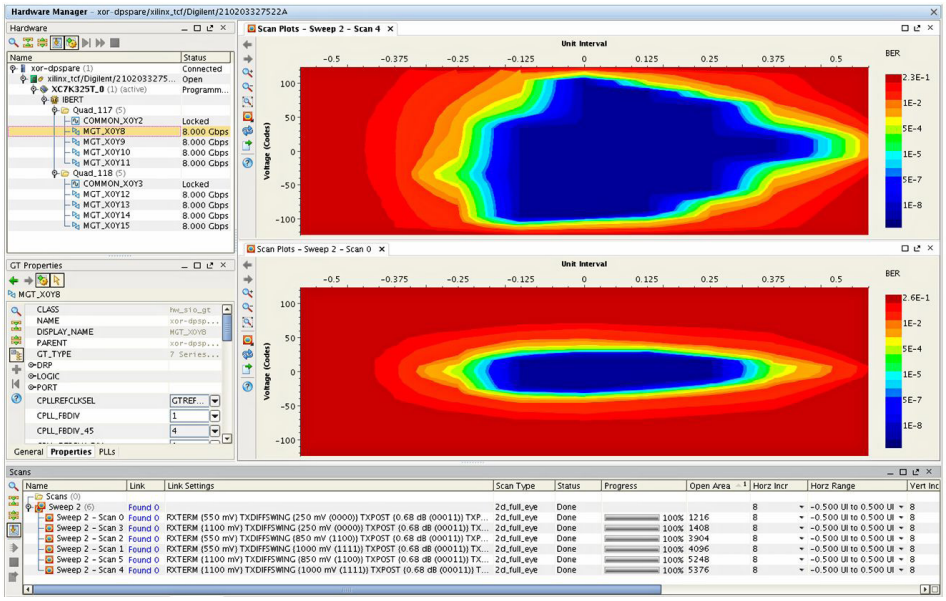
Benefits include:

- The ability to perform simple peek and poke operations on peripherals in the design
- The ability to write test patterns into memory without recompilation
- The ability to test and calibrate IP via an AXI interface
- The ability to check data inside of any AXI peripheral device

Integrated Serial I/O Analyzer

The Vivado Serial I/O Analyzer provides a fast, easy, and interactive way to set up and debug the high-speed serial I/O channels that are increasingly common in FPGA-based system designs. The Vivado Serial I/O Analyzer can perform bit-error-ratio (BER) measurements on multiple high-speed serial I/O channels and adjust high-speed serial transceiver parameters in real-time while these serial I/O channels are operating. The link-based Vivado Serial I/O Analyzer allows you to connect from any Transceiver transmitter (TX) to any Transceiver receiver (RX) in a system. Moreover, the TX and RX need not have the same SerDes architecture. The Vivado Serial I/O Analyzer also has the ability to automatically detect links and allows developers to create custom links, perform 2D eye scans, and sweep transceiver parameters in real-time as shown in Figure 11.

FIGURE 11: THE VIVADO SERIAL I/O ANALYZER



Reason 9: Accelerate Verification by >100X with C, C++, and SystemC

As discussed above, the Vivado Design Suite System Edition includes Vivado HLS, which allows your design team to quickly create and iterate algorithm designs in C, C++, and SystemC and to leverage the high simulation speed of these high-level programming languages for verification. Using Vivado HLS fixed-point and industry-standard floating-point math.h libraries, developers can rapidly model and iterate their designs using C functional specifications and can then create a target-aware RTL architecture based on simple clock-period and throughput considerations. Using C, C++, and SystemC as the initial design and modeling language greatly accelerates simulations (which run thousands of times faster than RTL simulations). In one video design example, a simulation of ten processed video frames ran approximately 12000 times faster in C than in HDL, as shown in Table 2.

TABLE 2: THE VIVADO DESIGN SUITE ACCELERATES DESIGN SIMULATION BY 12,000X IN THIS VIDEO EXAMPLE

Input	RTL Simulation Time	C Simulation Time	Acceleration
10 frames of video data	~2 days	10 Seconds	~12,000X

Conclusion

The Xilinx Vivado Design Suite delivers an SoC-strength, IP-centric and system-centric, generation-ahead development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation. This suite of design tools is designed for system-design teams that need to fit more system functions into fewer devices while increasing system performance, reducing system power, and lowering BOM cost.

To meet these objectives, the Vivado Design Suite is the ideal system-design tool for the following nine reasons:

- Vivado Design Suite allows you to push the device-density envelope farther
- Vivado Design Suite delivers robust performance and low power with predictable results
- Vivado Design Suite delivers unparalleled run time and memory utilization
- Vivado HLS lets you quickly generate IP using descriptions written in C, C++, or SystemC
- Vivado Design Suite supports model-based DSP design integration using Simulink and MATLAB from the MathWorks.
- Vivado IP Integrator shatters the RTL design-productivity barrier
- Vivado Integrated Design Environment provides a unified IDE for Design and Simulation
- Vivado Design Suite provides comprehensive hardware debug
- Vivado HLS accelerates verification by >100X using C, C++ or SystemC

Shouldn't your development team be taking advantage of the Vivado Design Suite today?

Take the NEXT STEP

To learn more about how the Vivado Design Suite is accelerating design productivity and a free 30-day evaluation of the Design Suite and Vivado High Level Synthesis please visit **www.xilinx.com/vivado**

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe
Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan
Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.
Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

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